

QUIZ 2: Design Your Own Solar Cell: Optimizing \$/W

Introduction

For this quiz, we'll be making our own solar cells. The quiz will be split up into 3 sections over 3 weeks: design, fabrication, and analysis. The goal is to minimize the dollars per watt (\$/W) of your cell, and a small fraction of your grade will be decided by this metric. The first section (outlined below) describes the different processes that go into the fabrication of a simple solar cell design. You're asked to choose between two different options for each processing step. The first deliverable, due 10/20, will be your selection of the different processing steps and a (short) justification as to your choices. The next week we'll be fabricating the cells in the lab, and will require your attendance in the laboratory to aid in the different steps. The third week will focus on the analysis and testing of the cells. You'll be able to measure the efficiency of your cell as well as use different analysis techniques to troubleshoot any efficiency-limiting issues in your cell.

Outline Of Fabrication Processes and Associated Costs

1. Si Wafer

Choosing a starting wafer for your process is probably one of the most influential factors on the final efficiency for your device. A material that is free of defects or impurities will result in a wafer that has a high minority carrier lifetime, and can lead to high efficiency, but will often cost much more. For this class, we have decided to just give you one choice of wafer, so we can focus on the different processing techniques to see how that affects the performance. The wafers provided will be high lifetime ($\tau > 10\mu\text{s}$) CZ-grown wafers, and will cost \$1 each.

2. Light Management

As outline in HW#1, the optical losses can be quite substantial. In order to maximize the number of photons that are absorbed by your device, surface texturing or an anti-reflection coating are often used. For light management, you'll be able to choose whether or not to use surface texturing. This will be done by using an alkaline chemical etch (KOH or NaOH.) The process results in a random pyramidal structure and can effectively increase the photon path length through the device and decrease

the reflectivity¹ (of note is figure 3.) The etch, which is an optional step, will be \$0.15 per wafer. We will etch for approx 40 minutes, according to the procedure provided by the paper in the footnote.

3. Phosphorous Diffusion

To create the emitter of your solar cell, you dope the surface layer with phosphorous, which creates a thin n-type layer. This process is done in a large furnace where silicon wafers are heated to very high temperatures in the presence of a phosphorous-bearing gas (POCl_3 .) The high temperatures allow the diffusion of phosphorous into the surface layer of the silicon wafer. This process can take several hours and is an expensive step of the processing. A longer diffusion process will create a deep n-type layer or emitter, while a short diffusion process will result in a shallow n-type layer or emitter. The depth of your emitter has an impact on the impurity gettering that occurs during the cool-down process after diffusion. Impurity gettering during cool-down allows many of the metal impurities present in your wafer to be “sucked up” by the emitter where they are less detrimental and results in a higher minority carrier lifetime. The emitter depth is often estimated by measuring the resistance of the surface layer. A thick emitter will have a lower resistance (recall the $1/\text{thickness}$ dependence on resistance of a thin film) while a shallow emitter will have a high resistance. You will have two options for emitter thickness, with the advantages for each approach listed below:

- Deep emitter (**30 Ohms/sq**)
 - o Improved gettering of metal impurities
 - o Lower resistance on surface layer, can decrease series resistance
 - o A thick layer will help prevent against shunts forming from front contacts that can spike through the emitter and effectively short-circuits the junction.
- Shallow emitter (**80 Ohms/sq**)
 - o Increased IQE of short wavelengths, which can lead to a larger J_{sc} .
 - o Cheaper: a shorter diffusion time decreases process time and reduces the energy costs per wafer (running a furnace uses a lot of electricity!)

A shallow emitter will cost \$1 while a deep emitter will cost \$1.50.

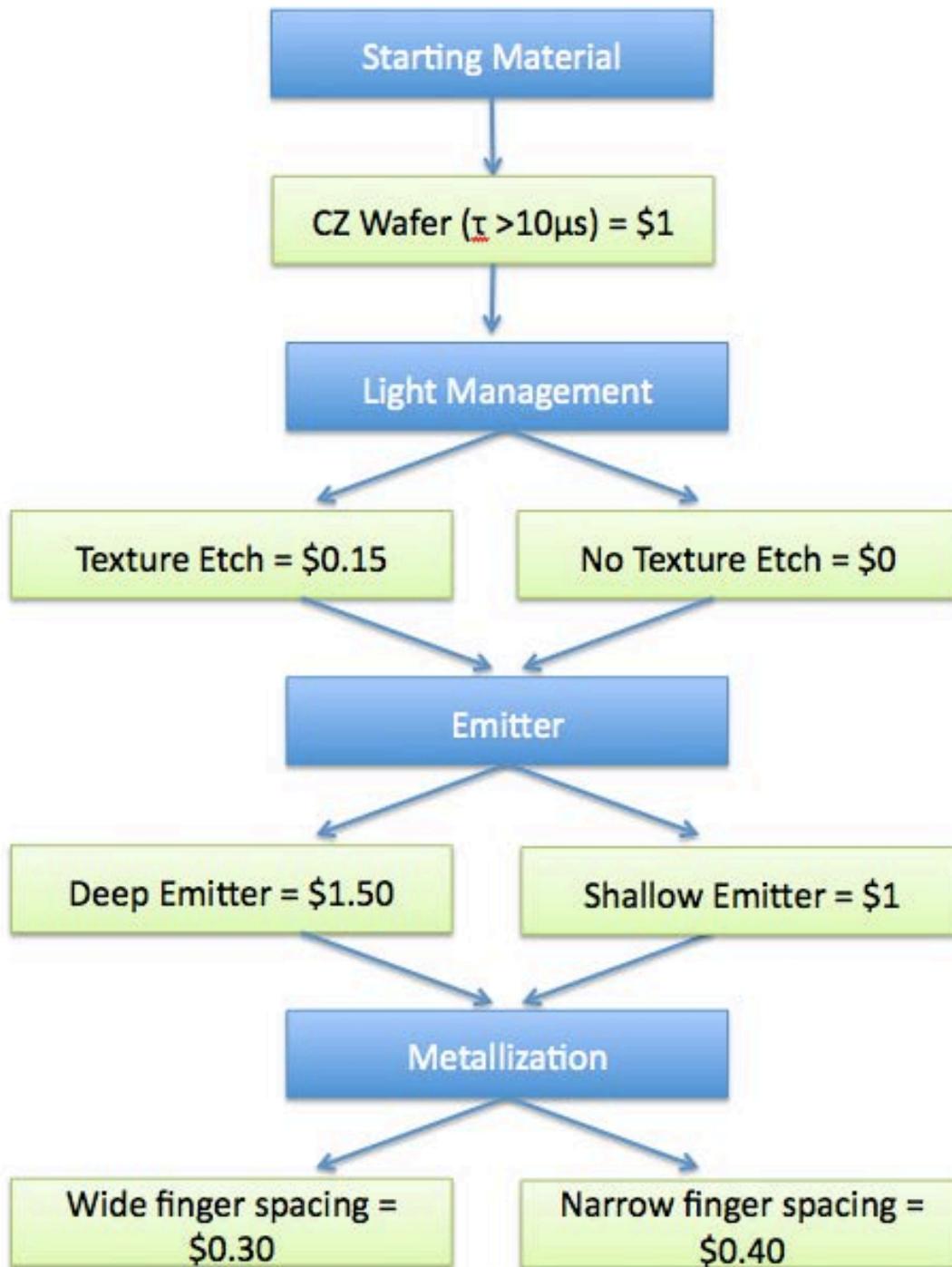
4. Metallization

The final step will be to put the front and back contacts onto our solar cell. This process involves screen-printing a paste that contains small metal particles onto the front and back surfaces of the wafer. After the screen printing, the wafers are fired in a furnace that reaches temperature $>800\text{C}$ for less than 8 seconds. This process allows the metal particles to form a completely interconnected network of metal and forms an Ohmic contact with the front and back surfaces. A good Ohmic contact is formed because some of the metal atoms diffuse into the surface layer. If the metal

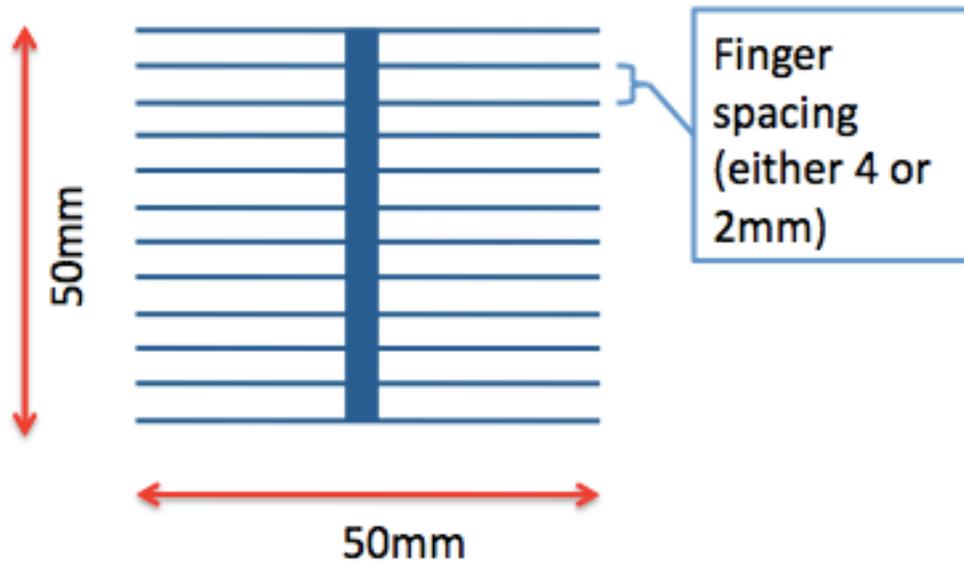
¹ P.K. Singh, R. Kumar, M. Lal, S.N. Singh, B.K. Das, *Solar Energy Materials & Solar Cells*, **70**, 103 (2001)

atoms diffuse to a depth that is deeper than the emitter, you form a shunt (as mentioned in process step 3.) For the metallization, you'll have two options for your finger spacing on your front contact. One option is to use fingers that are spaced 2mm apart, and the other is to use ones that are 4mm apart. Closer finger spacing will decrease the series resistance losses, but increase the shadowing losses, while the wider finger spacing decreases shadowing and increases series resistance losses. Because adding more fingers increases the amount of silver paste used, narrow finger spacing is a slightly more expensive option at \$0.40 per wafer as opposed to \$0.30 per wafer for wider spacing. Diagrams indicating the front contact patterns are presented on the following pages.

Flow Chart for Fabrication Process



Front Contact Pattern



QUIZ 2.1 Deliverable (Due 10/20)

The following questions should be completed and handed in during class on 10/20. Clearly, the information given is not perfect or complete, so make an educated guess as to what the best parameters will be! Each step also affects subsequent steps as well, so please elaborate on any interactions. There are no “right” answers here. We mainly want to see some good reasoning behind all your educated guesses. This deliverable is only worth 20% of the quiz grade, so don't fret too much about it! Remember, we are optimizing for \$/W, not efficiency! Busbar widths are 1.5mm and fingers are 150 microns wide.

Question 1:

- A) Please indicate if you would like to perform a surface texturing etch.
- B) Justify your selection by providing a rough, back-of-the-envelope calculation that estimates the relative increase in J_{sc} for your cell with and without a chemical etch. Indicate (briefly) how you think this affects your cost to efficiency ratio (\$/W) and provide some estimate to this metric.

Question 2:

- A) Please indicate if you would like a deep or shallow emitter.
- B) Justify your selection briefly by weighing the impacts of impurity gettering, sheet resistance, and IQE of short-wavelengths. You may assume that the concentration of diffused phosphorous is around $1 \times 10^{21} \text{cm}^{-3}$.

Question 3:

- A) Please indicate your desired finger spacing for your cell.
- B) Justify your selection by making some estimate of series resistance losses in your cell and how that relates to your efficiency to cost ratio (\$/W). This answer depends on your selection of emitter depth as well.

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2.627 / 2.626 Fundamentals of Photovoltaics
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