3.15 Electrical, Optical and Magnetic Materials and Devices
Prof. Caroline A. Ross
Fall 2006

Problem Set 3 pn junctions, BJTs and MOS
Due: Wednesday Oct. 18, 2006
Reference: Pierret chapers 10,15,16

Note: The pn junction and BJT are included in Exam 1 on 11th Oct. Solutions to questions 1-2 will be posted on 4 Oct, and will not be graded. However, it is strongly recommended that you work on the problems for practice before looking at the solutions. Questions 3-5 on MOS are due Oct. 18th and will be graded.

1. a) For a pn junction, draw the electron and hole concentrations vs distance outside the depletion region in the case of no bias, forward bias, and reverse bias, explaining *briefly* the shapes of the graphs. (2-3 sentences)

b) Estimate the voltage you would need to apply to cause avalanche breakdown in a Si pn junction with N_D in the n-side = N_A in the p-side = 10^{15} cm^{-3}. Assume that avalanche breakdown occurs at a field of 10^5 V cm^{-1}, and state any other assumptions you make.

c) A BJT can be used to detect light by allowing the light to fall on the base region. How could you bias the two junctions in the BJT to get a good response to light? For your biasing scheme, draw the band structure and explain where the current(s) flow.

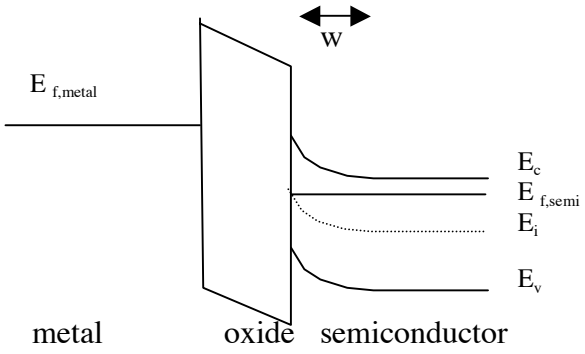
2. Consider a pnp bipolar junction transistor with an emitter doping level of 10^{18} cm^{-3}, a base doping level of 10^{16} cm^{-3}, and a collector doping level of 10^{15} cm^{-3}. The cross-sectional area of this device is 10^{-7} cm^2. The width of the base is W_B = 5 um, and $W_B < L_{DB}$ the minority carrier diffusion length in the base. Assume also that widths of the emitter and collector are much longer than minority carrier diffusion lengths in those regions.

(a) Sketch the equilibrium minority carrier concentration vs distance along the transistor from the emitter to the collector, in every region except for the depletion regions.

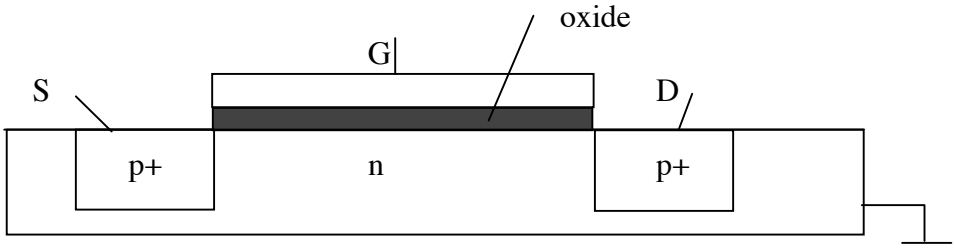
Voltages of V_{EB} = .3 volts and V_{CB} = -2 volts are now applied to the device.

(b) What regime of operation is the device in? What will be the *relative* values of I_E, I_B, and I_C, compared to one another?
(c) Sketch minority carrier concentration vs distance within the device, given the applied biases. Quantitatively label maximum and minimum concentrations within the emitter, base, and collector.
(d) Neglecting the length of the depletion region within the base, determine the current density flowing from the collector to the emitter, I_{CE}.
(e) If the polarity of V_{EB} were reversed, how would I_{CE} change (qualitatively)?

3. An ideal MOS junction is shown below. Band bending has caused the fermi level to touch the intrinsic level at the Si/SiO_2 interface.
a) Sketch the charge buildup, the electrostatic potential, and the electric field inside the semiconductor vs. position.
b) Do equilibrium conditions prevail inside the semiconductor? Sketch the electron concentration vs. distance inside the semiconductor.

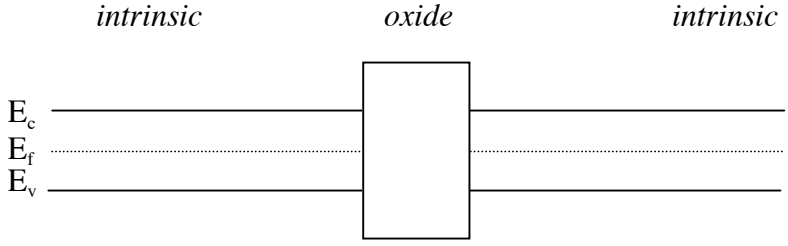


4. A MOSFET has the following structure:



a) What happens when you apply a voltage V_G to G (when S and D are grounded)? Consider both positive and negative voltages. Illustrate with a sketch of the MOS band diagram.
b) What happens when you apply a negative voltage V_D to D, for different values of V_G (zero, positive and negative)? (assume S is grounded.) Draw plots of current I_{SD} vs V_D for different values of V_G.

5. A semiconductor-oxide-semiconductor (SOS) structure can be built similar to a MOS structure. You can assume that all the bands are flat in the SOS structure when the semiconductor is intrinsic, so it looks like this:



a) Suppose now that one layer is p-type and the other is n-type. Draw the SOS band structure at equilibrium showing what is different compared to the picture above.
b) Redraw the band structure under bias (in both directions).
c) Explain what currents or carrier distributions might be expected in the device under these three bias conditions.