

1 Objective

This project will introduce you to the art of designing high speed frequency dividers. Your goal will be to design a divide-by-32/33 prescaler, as shown in Figure 1, that supports a minimum input frequency of 5 GHz with maximum power dissipation of 10 mW. Calculation of power dissipation must include all blocks in Figure 1 (including bias sources) except for input voltage sources V_{in} and V_{in} . You should strive to exceed one of these specifications such that

- You achieve an input frequency higher than 5 GHz with power dissipation not exceeding 10 mW, OR
- You achieve power dissipation less than 10 mW with an input frequency equal to or above 5 GHz.

In other words, you should explore either a high speed or low power approach under the given constraints.

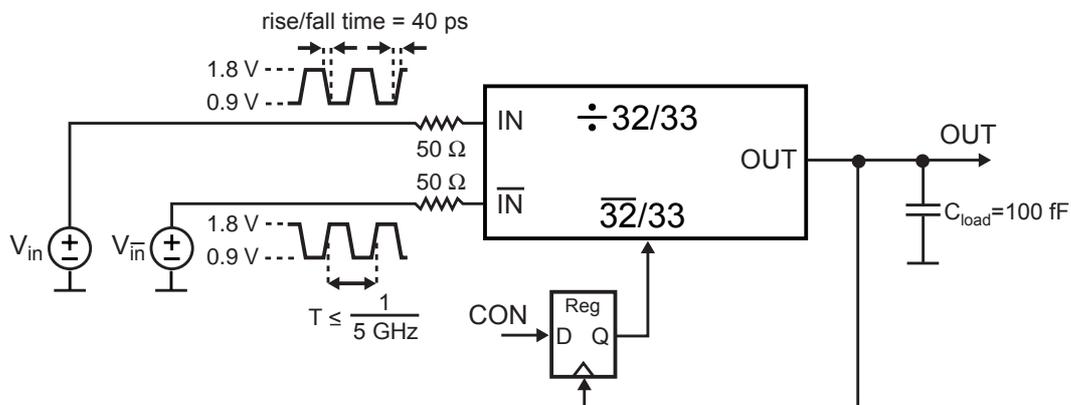


Figure 1: High Speed Divide-by-32/33 Circuit.

2 Report

Your report should consist of the sections described below. Note that one report is turned in for each project team (consisting of exactly 2 people), and must be no longer than 15 pages including all plots and figures.

- A brief introduction of the project and a statement of your overall goal (i.e., a high speed or low power divider design)
- A brief summary of the performance you achieved, which includes a table of the values you obtained for the following specifications (assume a temperature of 25 degrees Celsius except where otherwise stated):
 1. Maximum input frequency of overall divider
 - At 25 degrees Celsius
 - At 0 degrees Celsius
 - At 80 degrees Celsius
 2. Maximum input frequency achieved by each major section of the divider (i.e., the front end divider circuit, the differential-to-full swing circuit (if used), and the back end divider circuits)
 3. Total power dissipation (including bias sources)
 4. A breakdown of power dissipation in the divider (i.e., list the power consumed for each major block in the divider)
 5. Overall speed/power metric for the entire divider (i.e., Maximum speed (GHz)/Power dissipation (mW))
- A brief summary of simulated results that includes Hspice plots of the divider input and each divider stage output at the highest working frequency (with temperature set to 25 degrees Celsius). The plots must clearly show both the divide-by-32 and divide-by-33 operations as part of the same simulation run (i.e., you must switch the value of division during the simulation).
- A brief summary of the merits of your approach, which includes the following two sections:
 - The benefits and shortcomings of your architectural approach to the divider (i.e, why is it good for attaining high speed, or low power operation?) Also, explain the bottleneck in your architecture that prevents achievement of even higher input frequencies.
 - A brief description of the function and performance tradeoffs for each circuit block. (Example: first stage performs such and such operation, and was designed for high speed by doing so and so. Power dissipation was minimized by doing so and so.)

- A brief, qualitative summary of the impact of temperature variations on the divider performance. Specifically, is the performance better or worse at low and high temperatures, and why? (Note that the quantitative impact of temperature variations on divider speed is specified in the specification table described above.) In practice, one would also need to account for variations in transistor performance (i.e., using slow and fast models) and for resistor variations (typically $\pm 20\%$), but we will ignore these issues in this project for the sake of simplicity.
- Conclusion

3 Constraints

The following constraints must be met when stating results of your divider performance

- The model file `/mit/6.976/Models/0.18u/mos018.mod` must be used when simulating NMOS and PMOS devices
- Minimum length of all devices is $0.18\ \mu\text{m}$, and minimum width should be assumed to be $0.5\ \mu\text{m}$. (Note that the actual process would allow smaller widths, but these wouldn't be practical if wiring capacitance was included (i.e., the overall capacitance would then be dominated by the wires). We are not considering wire capacitance in this project, but we do want to be realistic in our consideration of its impact on sizing)
- Source and drain junction capacitances must be included for all transistors by specifying the perimeter and areas of each source/drain junction. You should use `hspc` for this as described on page 6 of the `hspc` manual (at <http://www-mtl.mit.edu/research/perrottgroup/tools.html>), where `hdin` = $0.4\ \mu\text{m}$, `hdout` = $0.5\ \mu\text{m}$, and a four sided perimeter should *not* be assumed. You are free to make use of fingers (as specified by the `m` and `geo` parameters) to reduce the impact of junction capacitance.
- Capacitance associated with poly resistors (in SCL logic) must be included in the simulation. The overall capacitance of a given resistor, C_p , is calculated based on its area and perimeter values, which are set by its resistance value and the required average current it must handle. Given the area and perimeter of the resistor, the overall capacitance is then calculated using the area and perimeter capacitances of poly over field (i.e., substrate).

To perform the above calculations, the relevant parameters for unsilicided P-doped poly (which will be assumed to be used for resistors in this project) are

- Area capacitance from poly to field: $100\ \text{aF}/\mu\text{m}^2$
- Fringe capacitance from poly to field: $50\ \text{aF}/\mu\text{m}^2$
- Sheet resistance of poly: $150\ \text{Ohms/square}$
- Electromigration rule for poly: $\leq 1\ \text{mA}/\mu\text{m}$ (applies to average current)

- Minimum poly width/length for resistors is $0.5 \mu\text{m}$ (to avoid dogbone layout of resistors when contacts are included)

Finally, a distributed model should be assumed for the impact of the total resistor capacitance, C_p , as shown in Figure 2.

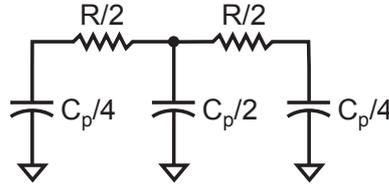


Figure 2: Modeling of distributed capacitance for resistor load.

- The maximum supply voltage is 1.8 Volts.
- The input to the divider is assumed to consist of two signal sources with 50Ω source resistances, V_{in} and $V_{\overline{in}}$, which are 180 degrees out of phase from one another and have the following properties

$$V_{high} = 1.8 \text{ V}, V_{low} = 0.9 \text{ V}, \text{risetime} = 40 \text{ ps}, \text{falltime} = 40 \text{ ps}$$

Note that 5 GHz versions of these signals can be achieved using the hspc program with the following lines

```
% timing 0n 40p 100p 0.9 1.8
% input vin [set 1 0 R]
% input vinb [set 0 1 R]
```

- The output to the divider must drive a load capacitance of 100 fF and a register that clocks in the CON signal (on either its rising or falling edge — your choice) as shown in Figure 1.
- You are allowed one ideal current source of any value that you choose (you must include its power dissipation when specifying the overall power dissipation of the divider). The source may be hooked between any nodes of your choice so long as one of the nodes is V_{dd} or ground.
- Inductors can *not* be used in this project (in practice, they yield better performance at the cost of significant die area).

4 Grading

The project will be graded as follows

- Understanding (10 %) — does your description of the architecture and circuits reveal that you understand the basic principles of designing a divide-by-32/33 circuit? Why did you choose the architecture, the type of logic style that was used in different parts of the divider, and did you clearly state the bottlenecks to achieving better performance?
- Originality (20 %) — is your divider implemented in a unique way that offers some particular advantage?
- Performance (30 %) — how fast does your divider operate (if speed was your goal)? How much power does it consume (if low power was your goal)?
- Practicality (10 %) — Are there any issues that would prevent your design from being easily manufacturable?
- Description (20 %) — are the fundamental concepts of your design clearly explained? Are the advantages of using your approach clearly spelled out? Is your writeup concise and to the point?
- Simulation (10 %) — did you adequately verify the performance of your design?

5 Suggested Design Procedure

Determine the achievable speed of a divide-by-2 configuration implemented with several different logic styles. Try to understand why some logic styles perform better than others. (A good, brief description comparing a few logic styles you tried and explaining the reasons for their performance differences will boost the grade you receive in the “Understanding” category.) Repeat this process for a divide-by-2/3 circuit.

Once you decide on logic styles for different parts of the divider, cascade the resulting divide-by-2/3 with divide-by-2 sections and then design the control qualifying logic to achieve proper timing of the control signal to the divide-by-2/3 stage. Verify that the control qualifying logic works properly by varying the divide value in a SPICE simulation and verifying that pulse swallowing occurs at the proper time.

Note that phase shifting techniques will achieve higher speed than gated approaches to the divide-by-2/3 implementation, but are much more difficult to design. I would suggest starting with a gated design, and then tackle phase shifting if you have the interest and time.