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High Speed Communication Circuits and Systems

Lecture 9

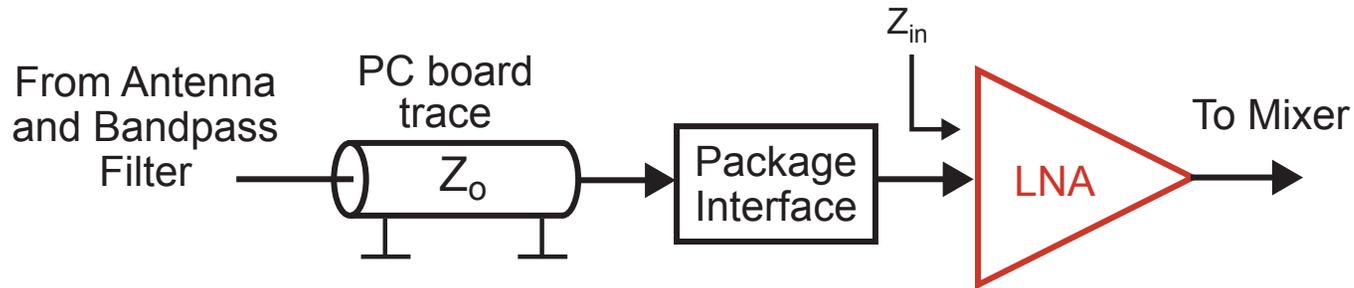
Low Noise Amplifiers

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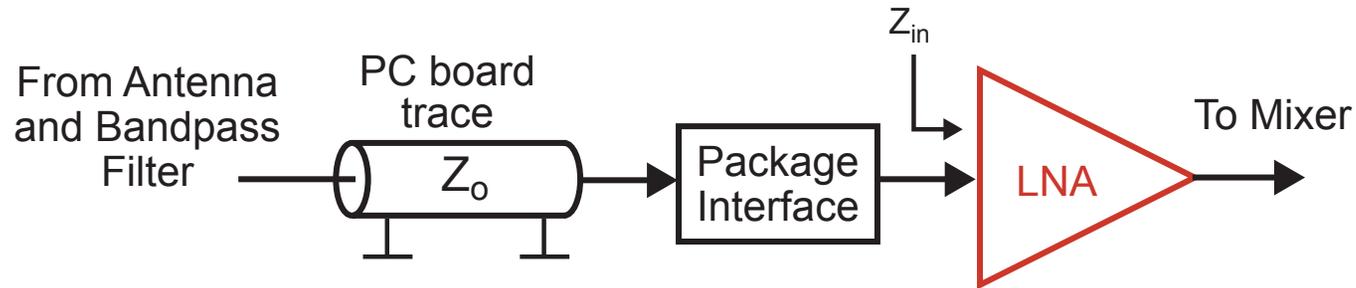
Narrowband LNA Design for Wireless Systems



■ Design Issues

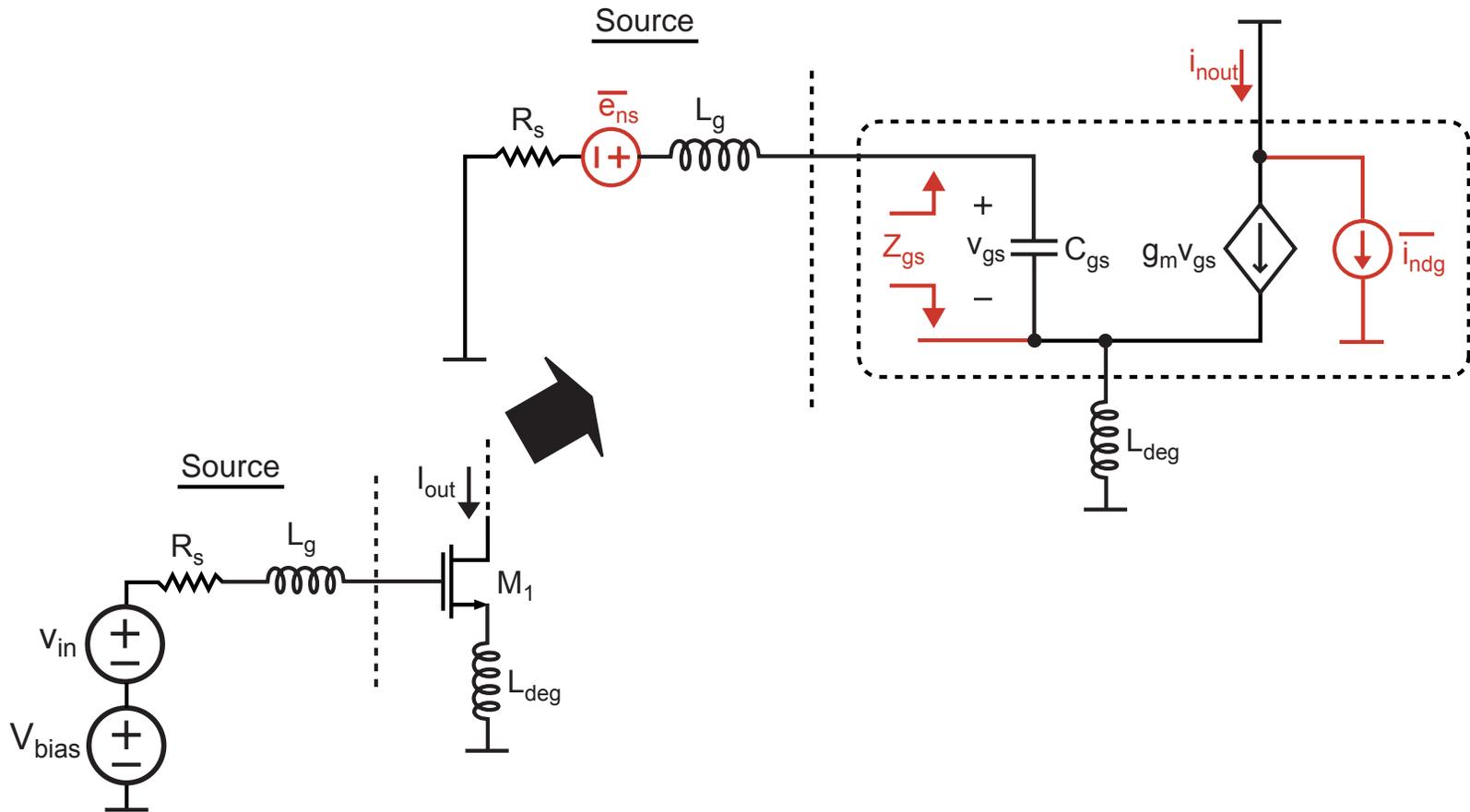
- Noise Figure – impacts receiver sensitivity
- Linearity (IIP3) – impacts receiver blocking performance
- Gain – high gain reduces impact of noise from components that follow the LNA (such as the mixer)
- Power match – want $Z_{in} = Z_o$ (usually = 50 Ohms)
- Power – want low power dissipation
- Bandwidth – need to pass the entire RF band for the intended radio application (i.e., all of the relevant channels)
- Sensitivity to process/temp variations – need to make it manufacturable in high volume

Our Focus in This Lecture



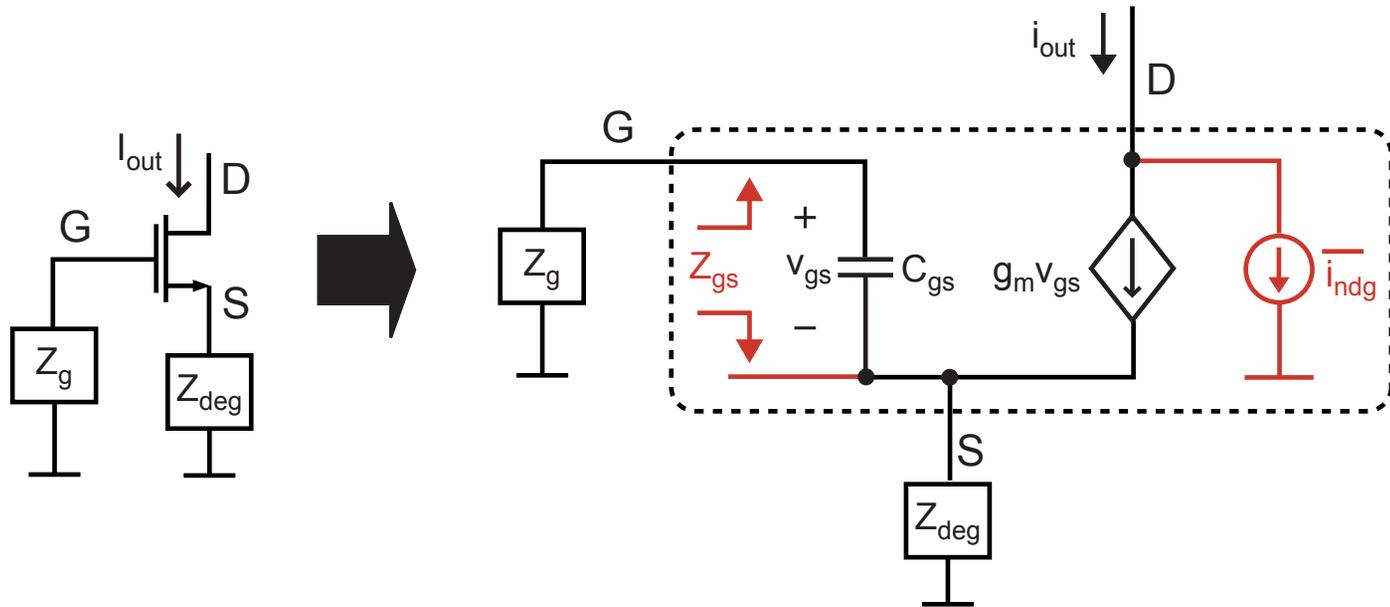
- Designing for low Noise Figure
- Achieving a good power match
- Hints at getting good IIP3
- Impact of power dissipation on design
- Tradeoff in gain versus bandwidth

Our Focus: Inductor Degenerated Amp



- Same as amp in Lecture 7 except for inductor degeneration
 - Note that noise analysis in Tom Lee's book does not include inductor degeneration (i.e., Table 11.1)

Recall Small Signal Model for Noise Calculations

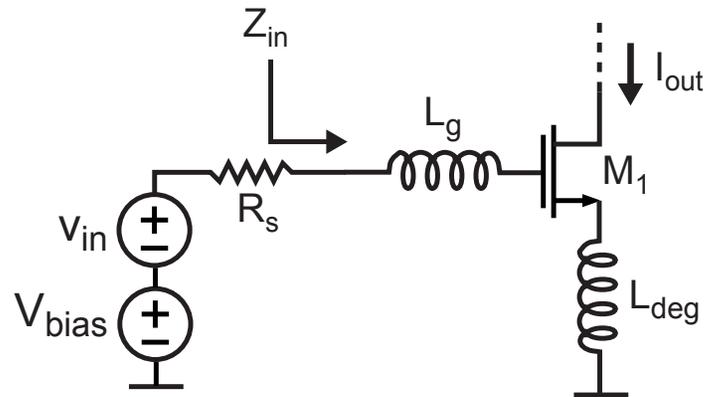


$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f} \left(|\eta|^2 + 2 \operatorname{Re} \{ c \chi_d \eta^* Z_{gsw} \} + \chi_d^2 |Z_{gsw}|^2 \right)$$

where: $\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{do}$, $\chi_d = \frac{g_m}{g_{do}} \sqrt{\frac{\delta}{5\gamma}}$, $Z_{gsw} = \omega C_{gs} Z_{gs}$

$$Z_{gs} = \frac{1}{sC_{gs}} \parallel \frac{Z_{deg} + Z_g}{1 + g_m Z_{deg}} \quad \eta = 1 - \left(\frac{g_m Z_{deg}}{Z_{deg} + Z_g} \right) Z_{gs}$$

Key Assumption: Design for Power Match



- Input impedance (from Lec 6)

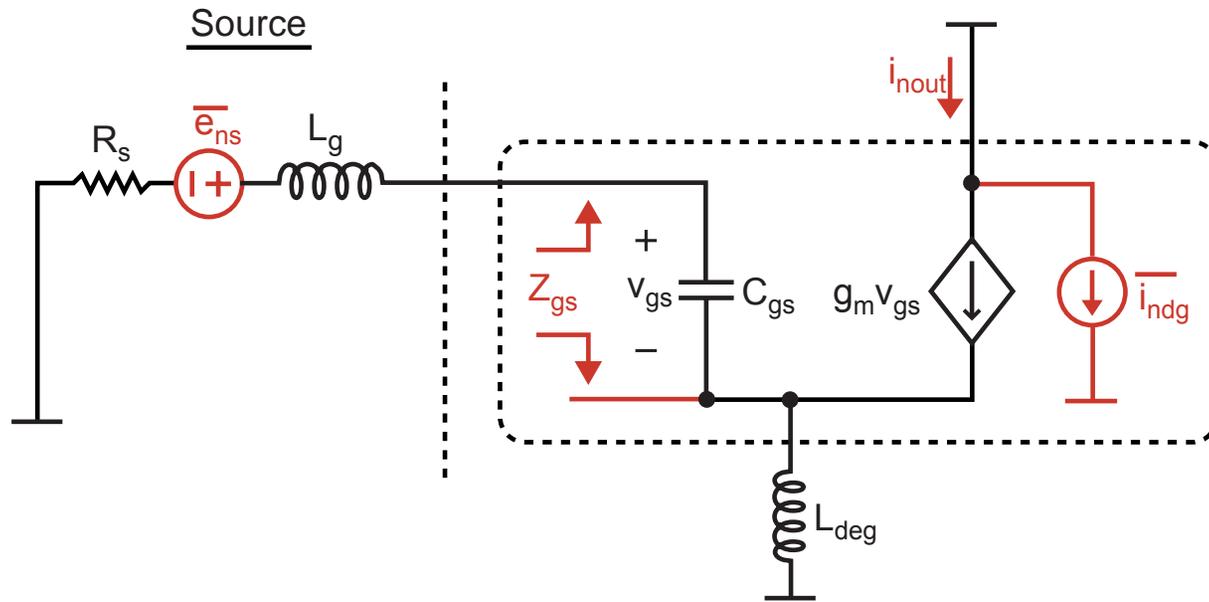
$$Z_{in}(s) = \frac{1}{sC_{gs}} + s(L_{deg} + L_g) + \frac{g_m}{C_{gs}}L_{deg}$$

Real!

- Set to achieve pure resistance = R_s at frequency ω_o

$$\Rightarrow \frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = \omega_o, \quad \frac{g_m}{C_{gs}}L_{deg} = R_s$$

Process and Topology Parameters for Noise Calculation



- **Process parameters**

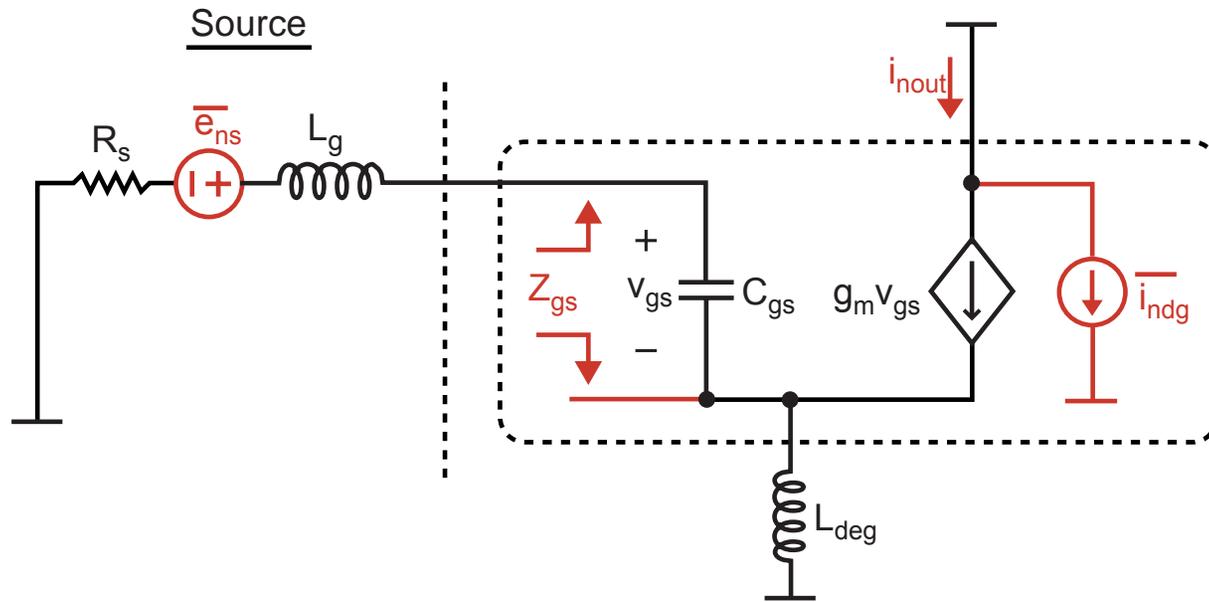
- For 0.18 μ CMOS, we will assume the following

$$c = -j0.55, \quad \gamma = 3, \quad \delta = 2\gamma = 6, \quad \frac{g_m}{g_{do}} = \frac{1}{2} \Rightarrow \chi_d = 0.32$$

- **Circuit topology parameters Z_g and Z_{deg}**

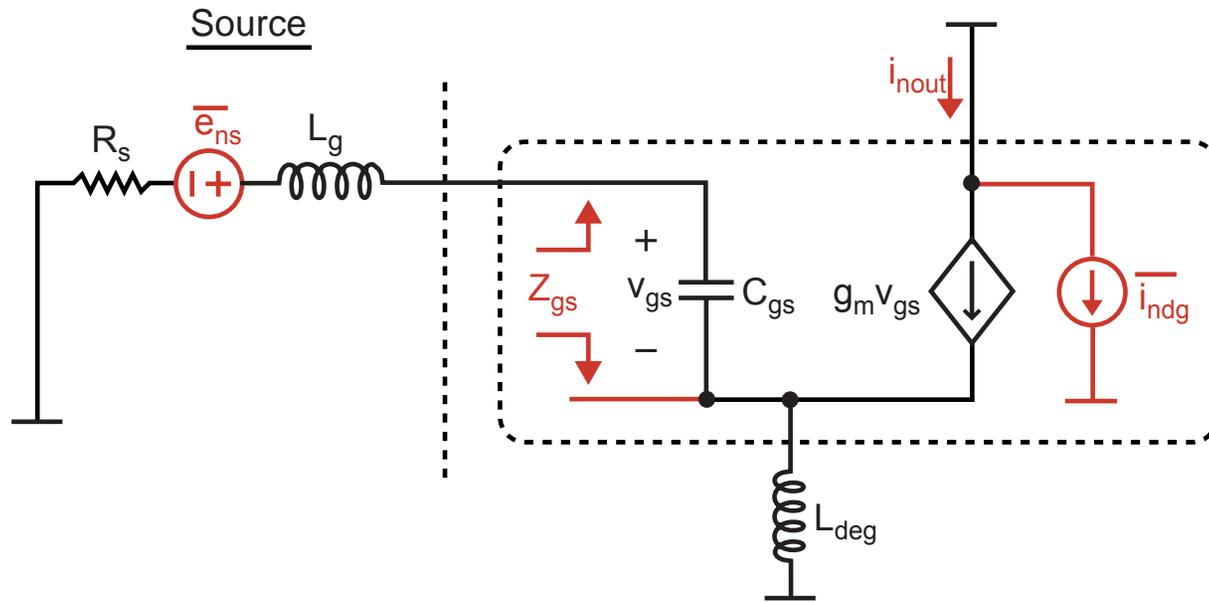
$$Z_g = R_s + j\omega L_g, \quad Z_{deg} = j\omega L_{deg}$$

Calculation of Z_{gs}



$$\begin{aligned}
 Z_{gs} &= \frac{1}{sC_{gs}} \parallel \frac{Z_{deg} + Z_g}{1 + g_m Z_{deg}} = \frac{1}{j\omega_o C_{gs}} \parallel \frac{j\omega_o(L_{deg} + L_g) + R_s}{1 + g_m j\omega_o L_{deg}} \\
 &= \frac{j\omega_o(L_{deg} + L_g) + R_s}{1 - \omega_o^2 C_{gs}(L_{deg} + L_s) + j\omega_o(g_m L_{deg} + R_s C_{gs})} \\
 &= \frac{j\omega_o(L_{deg} + L_g) + R_s}{j\omega_o(g_m L_{deg} + R_s C_{gs})}
 \end{aligned}$$

Calculation of η



$$\begin{aligned}
 \eta &= 1 - \left(\frac{g_m Z_{deg}}{Z_{deg} + Z_g} \right) Z_{gs} = 1 - \frac{g_m j \omega_o L_{deg}}{j \omega_o (L_{deg} + L_g) + R_s} Z_{gs} \\
 &= 1 - \frac{g_m j \omega_o L_{deg}}{j \omega_o (g_m L_{deg} + R_s C_{gs})} = 1 - \frac{(g_m / C_{gs}) L_{deg}}{\underbrace{(g_m / C_{gs}) L_{deg} + R_s}_{= R_s}} \\
 &= 1 - \frac{R_s}{R_s + R_s} = \boxed{\frac{1}{2}}
 \end{aligned}$$

Calculation of Z_{gsw}

- By definition

$$Z_{gsw} = w_o C_{gs} Z_{gs} \left(Q = \frac{1}{w_o C_{gs} 2R_s} = \frac{w_o(L_g + L_{deg})}{2R_s} \right)$$

- Calculation

$$Z_{gsw} = w_o C_{gs} \frac{jw_o(L_{deg} + L_g) + R_s}{jw_o(g_m L_{deg} + R_s C_{gs})}$$

$$= \frac{jw_o^2 C_{gs}(L_{deg} + L_g) + w_o C_{gs} R_s}{jw_o(g_m L_{deg} + R_s C_{gs})}$$

$$= \frac{j1 + 1/(2Q)}{jw_o(g_m L_{deg} + R_s C_{gs})}$$

$$= \frac{j1 + 1/(2Q)}{jw_o C_{gs} ((g_m / C_{gs}) L_{deg} + R_s)}$$

$$= \frac{j1 + 1/(2Q)}{jw_o C_{gs} (R_s + R_s)} = \frac{j1 + 1/(2Q)}{j1/Q} = \frac{1}{2}(2Q - j)$$

Calculation of Output Current Noise

- Step 3: Plug in values to noise expression for i_{ndg}

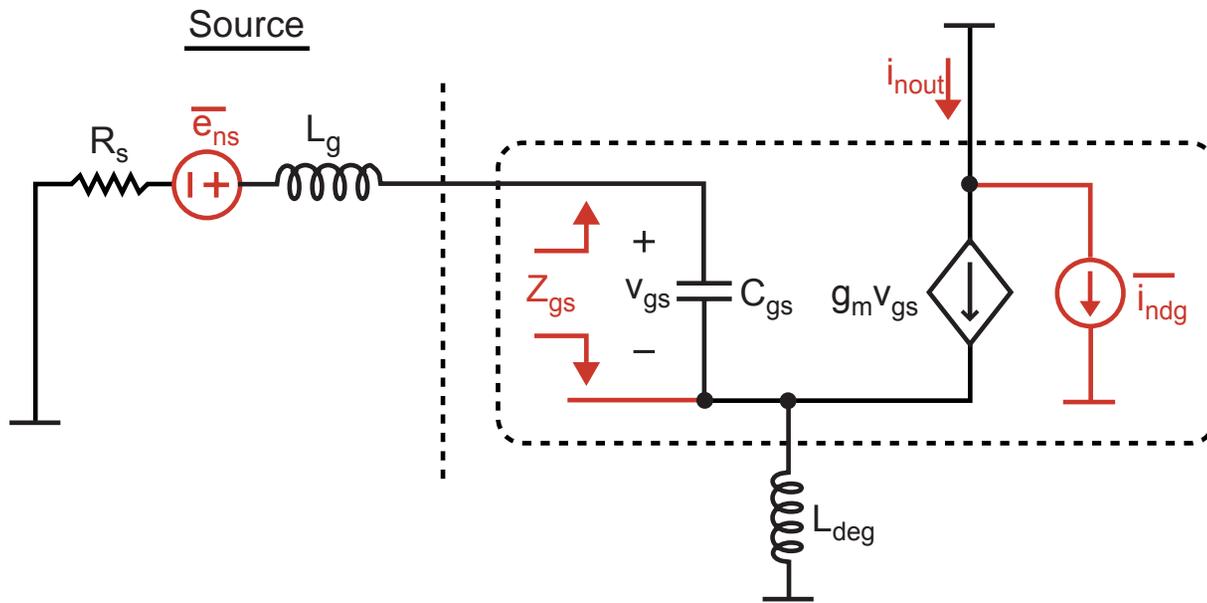
$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f} \left(|\eta|^2 + 2\text{Re} \left\{ -j|c|\chi_d\eta^* Z_{gsw} \right\} + \chi_d^2 |Z_{gsw}|^2 \right)$$

$$\text{where } \eta = \frac{1}{2}, \quad Z_{gsw} = \frac{1}{2}(2Q - j)$$

$$\Rightarrow \frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f} \left(\frac{1}{4} + 2\text{Re} \left\{ -j|c|\chi_d \frac{1}{4}(2Q - j) \right\} + \chi_d^2 \frac{1}{4} |2Q - j|^2 \right)$$

$$= \frac{\overline{i_{nd}^2}}{\Delta f} \frac{1}{4} \left(1 - 2|c|\chi_d + \chi_d^2(4Q^2 + 1) \right)$$

Compare Noise With and Without Inductor Degeneration



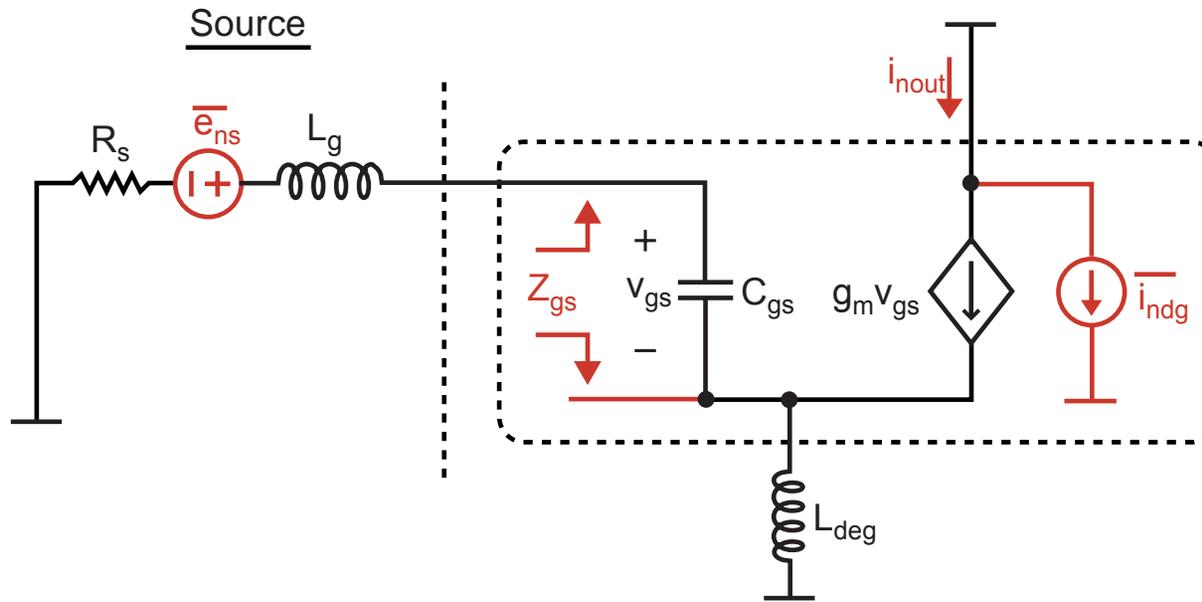
- From Lecture 7, we derived for $L_{deg} = 0$, $\omega_o^2 = 1/(L_g C_{gs})$

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f} \left(1 - 2|c|\chi_d + \chi_d^2(Q^2 + 1) \right)$$

- We now have for $(g_m/C_{gs})L_{deg} = R_s$, $\omega_o^2 = 1/((L_g + L_{deg})C_{gs})$

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f} \frac{1}{4} \left(1 - 2|c|\chi_d + \chi_d^2(4Q^2 + 1) \right)$$

Derive Noise Factor for Inductor Degenerated Amp

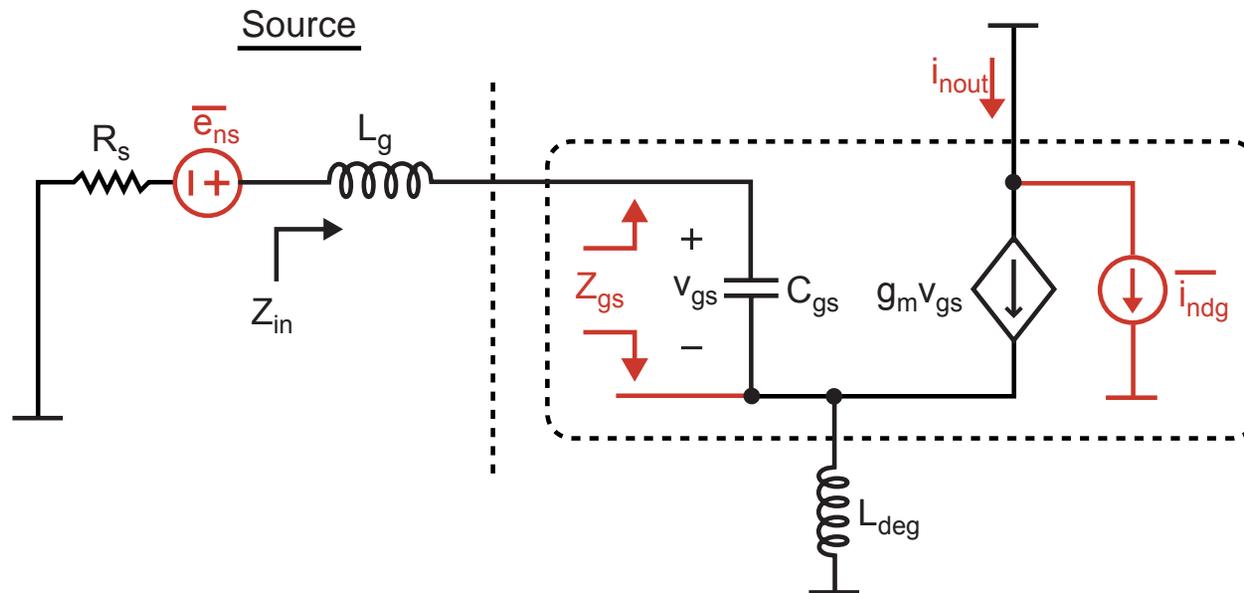


- Recall the alternate expression for Noise Factor derived in Lecture 8

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}} = \frac{\overline{i_{nout}^2(tot)}}{\overline{i_{nout}^2(in)}}$$

- We now know the output noise due to the transistor noise
 - We need to determine the output noise due to the source resistance

Output Noise Due to Source Resistance



$$Z_{in} = \frac{1}{j\omega_0 C_{gs}} + j\omega_0(L_{deg} + L_g) + \frac{g_m}{C_{gs}}L_{deg} = R_s$$

$$\Rightarrow v_{gs} = \frac{\overline{e_{ns}}}{R_s + Z_{in}} \left(\frac{1}{j\omega_0 C_{gs}} \right) = \frac{\overline{e_{ns}}}{2R_s} \left(\frac{1}{j\omega_0 C_{gs}} \right) = \left(\frac{Q}{j} \right) \overline{e_{ns}}$$

$$\Rightarrow i_{nout} = g_m \left(\frac{Q}{j} \right) \overline{e_{ns}}$$

$$\Rightarrow \overline{i_{nout}^2} = (g_m Q)^2 \overline{e_{ns}^2}$$

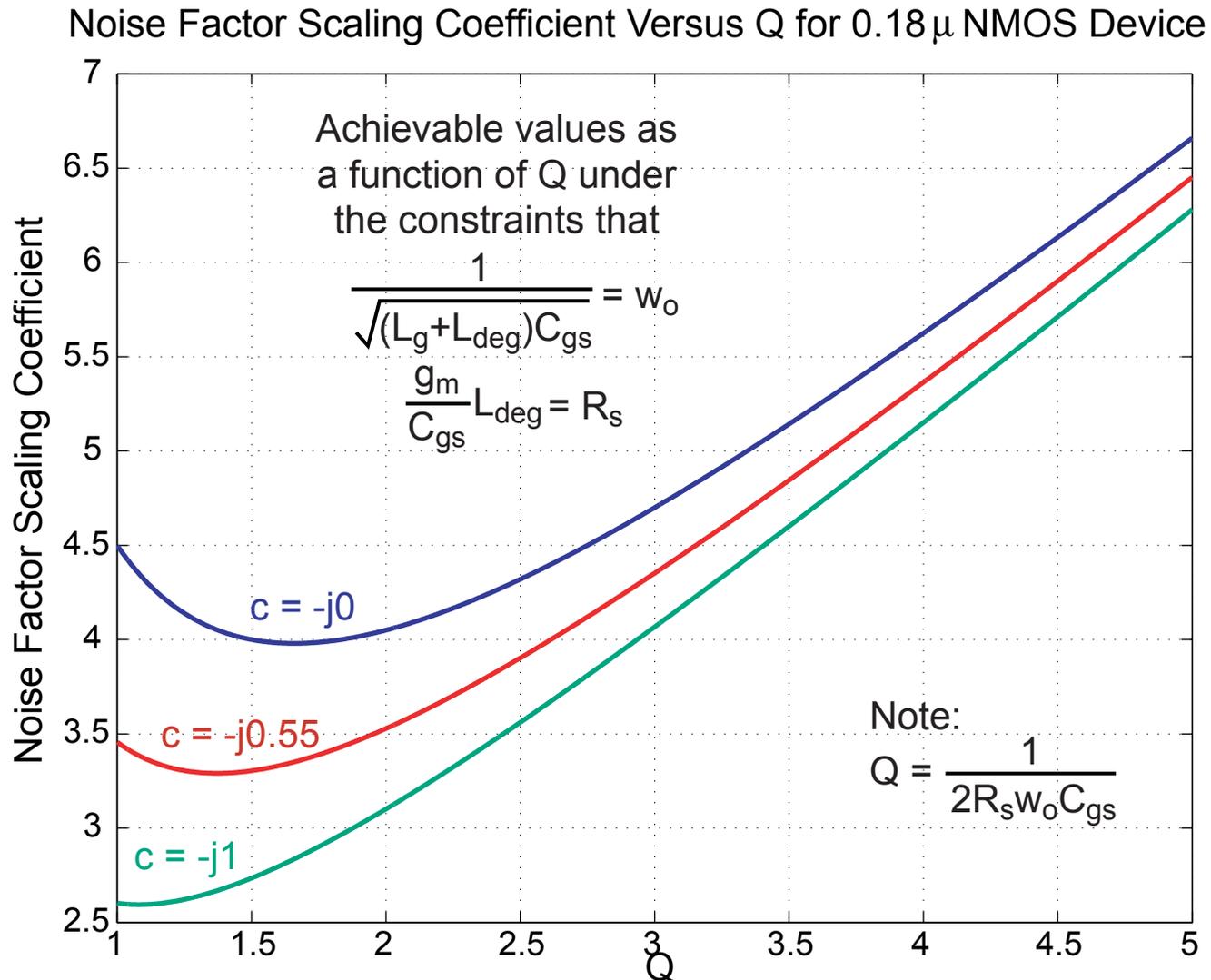
Noise Factor for Inductor Degenerated Amplifier

$$\begin{aligned}\text{Noise Factor} &= \frac{(g_m Q)^2 \overline{e_{ns}^2} + \overline{i_{ndg}^2} / \Delta f}{(g_m Q)^2 \overline{e_{ns}^2}} = 1 + \frac{\overline{i_{ndg}^2} / \Delta f}{(g_m Q)^2 \overline{e_{ns}^2}} \\ &= 1 + \frac{4kT \gamma g_{do} (1/4) (1 - 2|c| \chi_d + \chi_d^2 (4Q^2 + 1))}{(g_m Q)^2 4kT R_s} \\ &= 1 + \left(\frac{1}{g_m Q R_s} \right) \gamma \left(\frac{g_{do}}{g_m} \right) \frac{1}{4Q} (1 - 2|c| \chi_d + (4Q^2 + 1) \chi_d^2) \\ &= 1 + \left(\frac{2\omega_o R_s C_{gs}}{g_m R_s} \right) \gamma \left(\frac{g_{do}}{g_m} \right) \frac{1}{4Q} (1 - 2|c| \chi_d + (4Q^2 + 1) \chi_d^2)\end{aligned}$$

$$= 1 + \left(\frac{\omega_o}{\omega_t} \right) \gamma \left(\frac{g_{do}}{g_m} \right) \frac{1}{2Q} (1 - 2|c| \chi_d + (4Q^2 + 1) \chi_d^2)$$

Noise Factor scaling coefficient

Noise Factor Scaling Coefficient Versus Q



Achievable Noise Figure in 0.18μ with Power Match

- Suppose we desire to build a narrowband LNA with center frequency of 1.8 GHz in 0.18μ CMOS ($c=-j0.55$)
 - From Hspice – at $V_{gs} = 1$ V with NMOS ($W=1.8\mu$, $L=0.18\mu$)
 - measured $g_m = 871 \mu\text{S}$, $C_{gs} = 2.9$ fF

$$\Rightarrow \omega_t \approx \frac{g_m}{C_{gs}} = \frac{871 \times 10^{-6}}{2.9 \times 10^{-15}} = 2\pi(47.8\text{GHz})$$

$$\Rightarrow \frac{\omega_o}{\omega_t} = \frac{2\pi 1.8e9}{2\pi 47.8e9} \approx \frac{1}{26.6}$$

- Looking at previous curve, with $Q \approx 2$ we achieve a Noise Factor scaling coefficient ≈ 3.5

$$\Rightarrow \text{Noise Factor} \approx 1 + \frac{1}{26.6} 3.5 \approx 1.13$$

$$\Rightarrow \text{Noise Figure} = 10 \log(1.13) \approx 0.53 \text{ dB}$$

Component Values for Minimum NF with Power Match

- Assume $R_s = 50$ Ohms, $Q = 2$, $f_o = 1.8$ GHz, $f_t = 47.8$ GHz

- C_{gs} calculated as

$$Q = \frac{1}{2R_s\omega_o C_{gs}}$$

$$\Rightarrow C_{gs} = \frac{1}{2R_s\omega_o Q} = \frac{1}{2(50)2\pi 1.8e9(2)} = 442 \text{ fF}$$

- L_{deg} calculated as

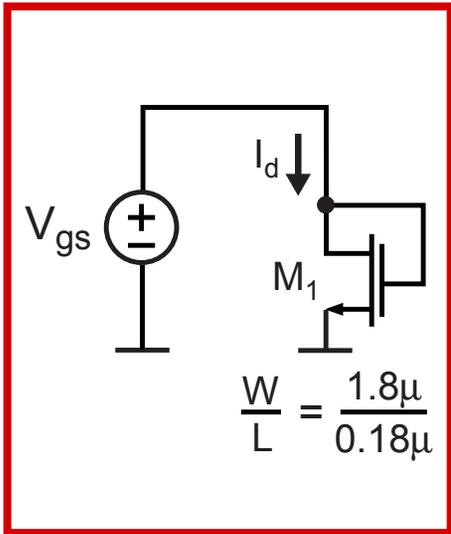
$$\frac{g_m}{C_{gs}} L_{deg} = R_s \Rightarrow L_{deg} = \frac{R_s}{\omega_t} = \frac{50}{2\pi 47.8e9} = 0.17 \text{ nH}$$

- L_g calculated as

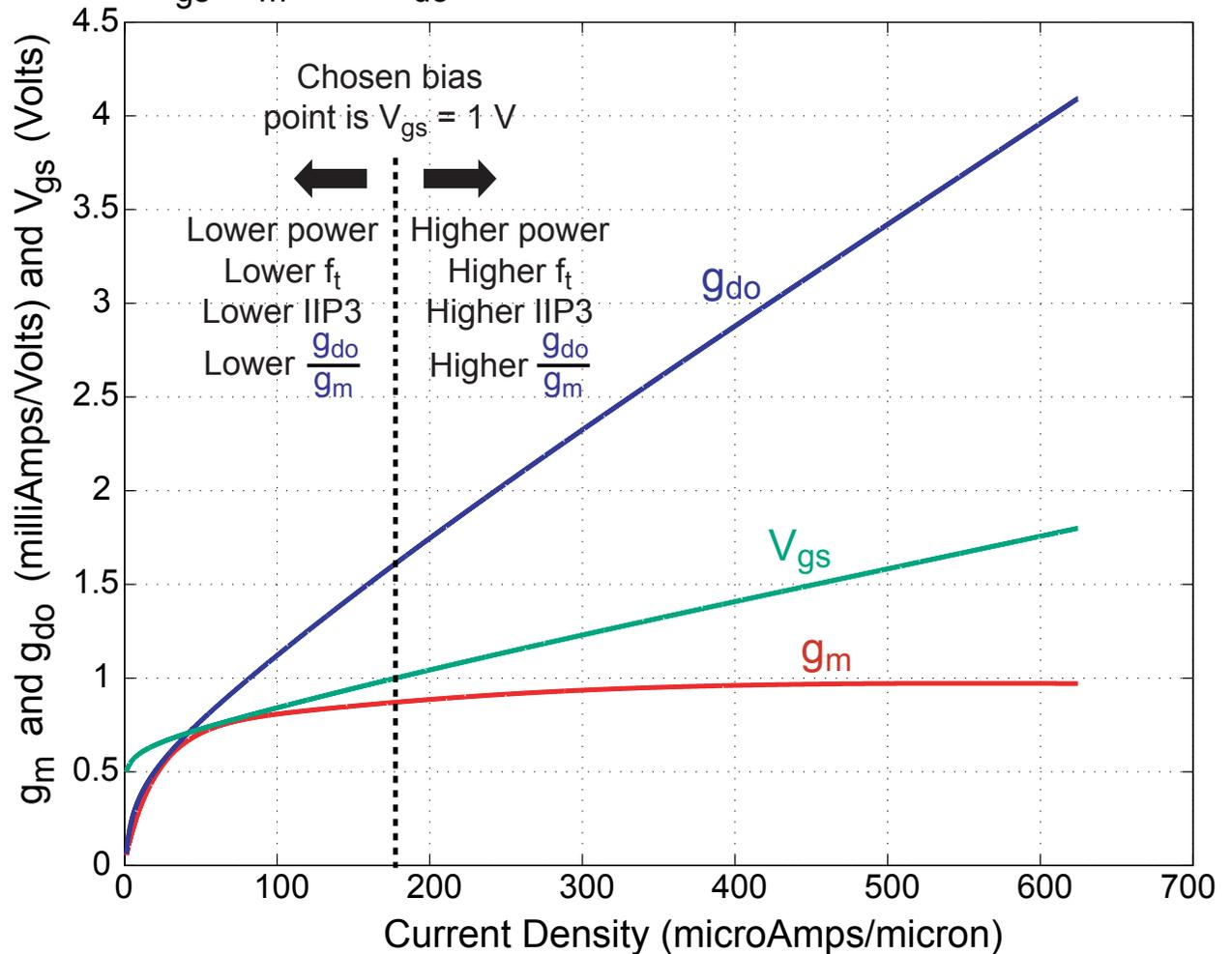
$$\frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = \omega_o \Rightarrow L_g = \frac{1}{\omega_o^2 C_{gs}} - L_{deg}$$

$$\Rightarrow L_g = \frac{1}{(2\pi 1.8e9)^2 442e-15} - 0.17e-9 = 17.5 \text{ nH}$$

Have We Chosen the Correct Bias Point? ($V_{gs} = 1V$)



V_{gs} , g_m , and g_{do} versus Current Density for $0.18\mu\text{NMOS}$



■ Note: IIP3 is also a function of Q

Calculation of Bias Current for Example Design

- Calculate current density from previous plot

$$V_{gs} = 1V \Rightarrow I_{dens} \approx 175\mu A/\mu m$$

- Calculate W from Hspice simulation (assume L=0.18 μm)

$$C_{gs} = 2.9fF \text{ for } W = 1.8\mu m \Rightarrow W = \frac{442fF}{2.9fF} 1.8\mu m \approx 274\mu m$$

- Could also compute this based on C_{ox} value
- Calculate bias current

$$I_{bias} = I_{den}W = (175\mu A/\mu m)(274\mu m) \approx 48mA$$

- Problem: this is not low power!!

We Have Two “Handles” to Lower Power Dissipation

- **Key formulas**

$$I_{bias} = I_{den}W$$

$$F = 1 + \left(\frac{w_o}{w_t}\right) \gamma \left(\frac{g_{do}}{g_m}\right) \frac{1}{2Q} \left(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2\right)$$

- **Lower current density, I_{den}**

- **Benefits**

⇒ lower power, lower $\frac{g_{do}}{g_m}$ ratio

- **Negatives**

⇒ lower IIP3, lower f_t

- **Lower W**

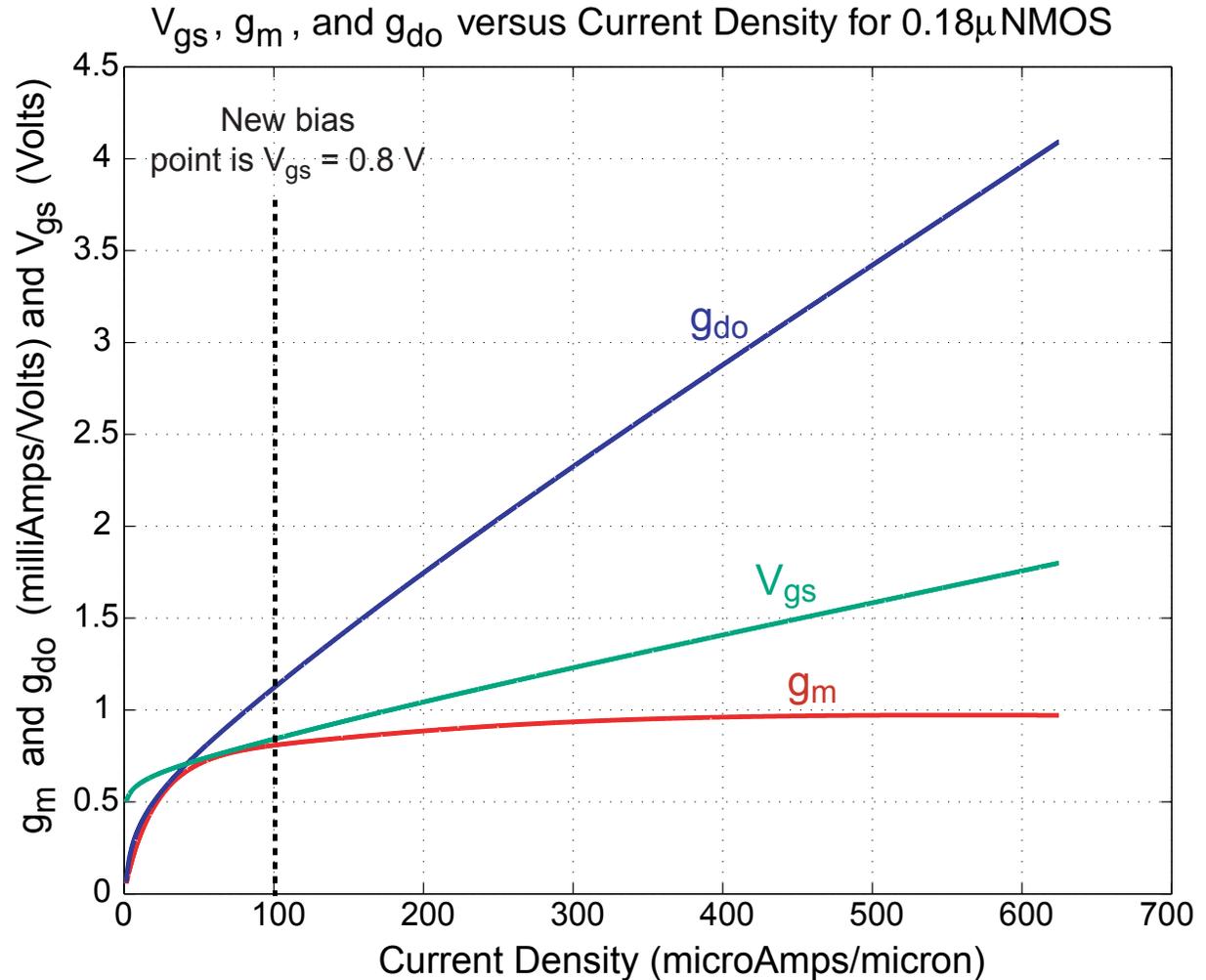
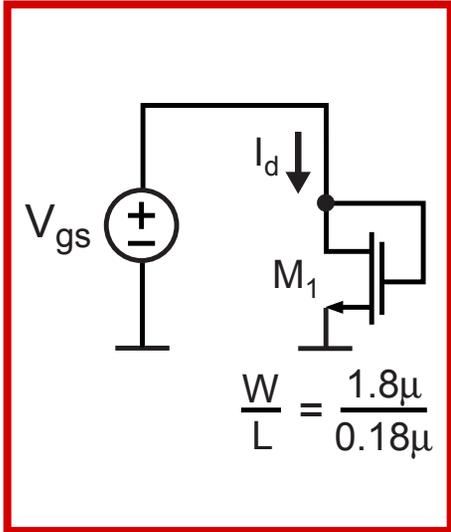
- **Benefit: lower power**

- **Negatives**

⇒ lower $C_{gs} = \frac{2}{3}WLC_{ox} \Rightarrow$ higher $Q = \frac{1}{w_o C_{gs} 2R_s}$

⇒ higher F (and higher inductor values)

First Step in Redesign – Lower Current Density, I_{den}



- Need to verify that IIP3 still OK (once we know Q)

Recalculate Process Parameters

- Assume that the only thing that changes is g_m/g_{do} and f_t
 - From previous graph ($I_{den} = 100 \mu A/\mu m$)

$$\frac{g_m}{g_{do}} \approx \frac{.78}{1.15} \approx 0.68 \Rightarrow \chi_d = \frac{g_m}{g_{do}} \sqrt{\frac{\delta}{5\gamma}} = 0.63 \sqrt{\frac{2}{5}} \approx 0.43$$

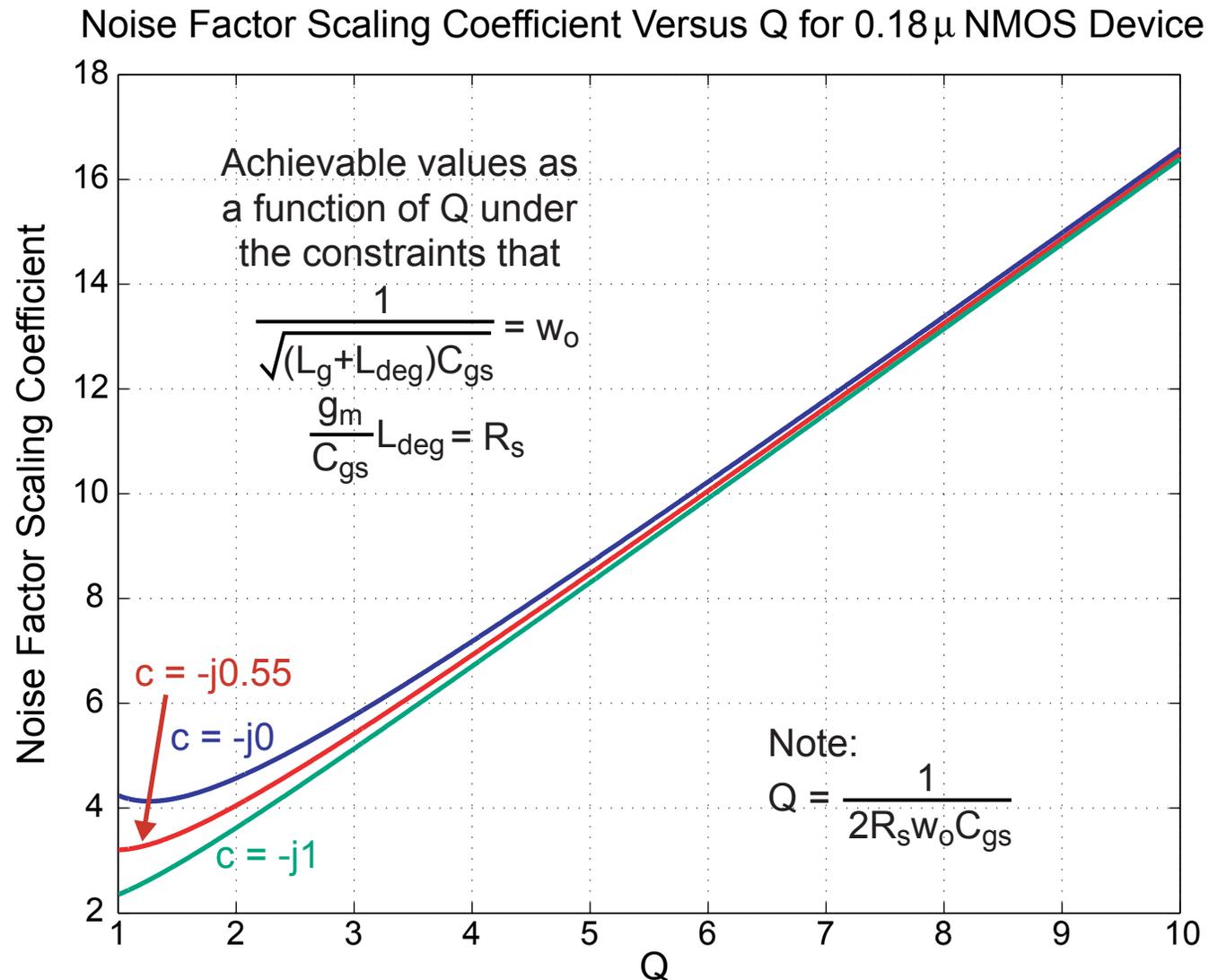
$$w_t \approx \frac{g_m}{C_{gs}} \approx \frac{0.78mS}{2.9fF} = (2\pi)42.8GHz$$

- We now need to replot the Noise Factor scaling coefficient
 - Also plot over a wider range of Q

$$F = 1 + \frac{\left(\frac{w_o}{w_t}\right) \gamma \left(\frac{g_{do}}{g_m}\right) \frac{1}{2Q} \left(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2\right)}{\hspace{10em}}$$

Noise Factor scaling coefficient

Update Plot of Noise Factor Scaling Coefficient



Second Step in Redesign – Lower W

- **Recall**

$$C_{gs} = \frac{2}{3}WLC_{ox}, \quad Q = \frac{1}{\omega_0 C_{gs} 2R_s}$$

- **I_{bias} can be related to Q as**

$$I_{bias} = I_{den}W = I_{den}\frac{3}{2LC_{ox}}C_{gs} = I_{den}\frac{3}{2LC_{ox}}\frac{1}{\omega_0 2R_s Q}$$

$$\Rightarrow I_{bias} \propto \frac{1}{Q}$$

- **We previously chose Q = 2, let's now choose Q = 6**

- **Cuts power dissipation by a factor of 3!**
- **New value of W is one third the old one**

$$\Rightarrow W = \frac{274fF}{3} \approx 91\mu m$$

Power Dissipation and Noise Figure of New Design

■ Power dissipation

$$I_{bias} = I_{den}W = (100\mu A/\mu m)(91\mu m) = 9.1mA$$

- At 1.8 V supply

$$\Rightarrow \text{Power} = (9.1mA)(1.8V) = 16.4mW$$

■ Noise Figure

- f_t previously calculated, get scaling coeff. from plot

$$\frac{\omega_o}{\omega_t} = \frac{2\pi 1.8e9}{2\pi 42.8e9} \approx \frac{1}{23.8}, \text{ scaling coeff. } \approx 10$$

$$\Rightarrow \text{Noise Factor} \approx 1 + \frac{1}{23.8}10 \approx 1.42$$

$$\Rightarrow \text{Noise Figure} = 10 \log(1.42) \approx 1.52 \text{ dB}$$

Updated Component Values

- Assume $R_s = 50$ Ohms, $Q = 6$, $f_o = 1.8$ GHz, $f_t = 42.8$ GHz

- C_{gs} calculated as

$$Q = \frac{1}{2R_s\omega_o C_{gs}}$$

$$\Rightarrow C_{gs} = \frac{1}{2R_s\omega_o Q} = \frac{1}{2(50)2\pi 1.8e9(6)} \approx 147 \text{ fF}$$

- L_{deg} calculated as

$$\frac{g_m}{C_{gs}} L_{deg} = R_s \Rightarrow L_{deg} = \frac{R_s}{\omega_t} = \frac{50}{2\pi 42.8e9} = 0.19 \text{ nH}$$

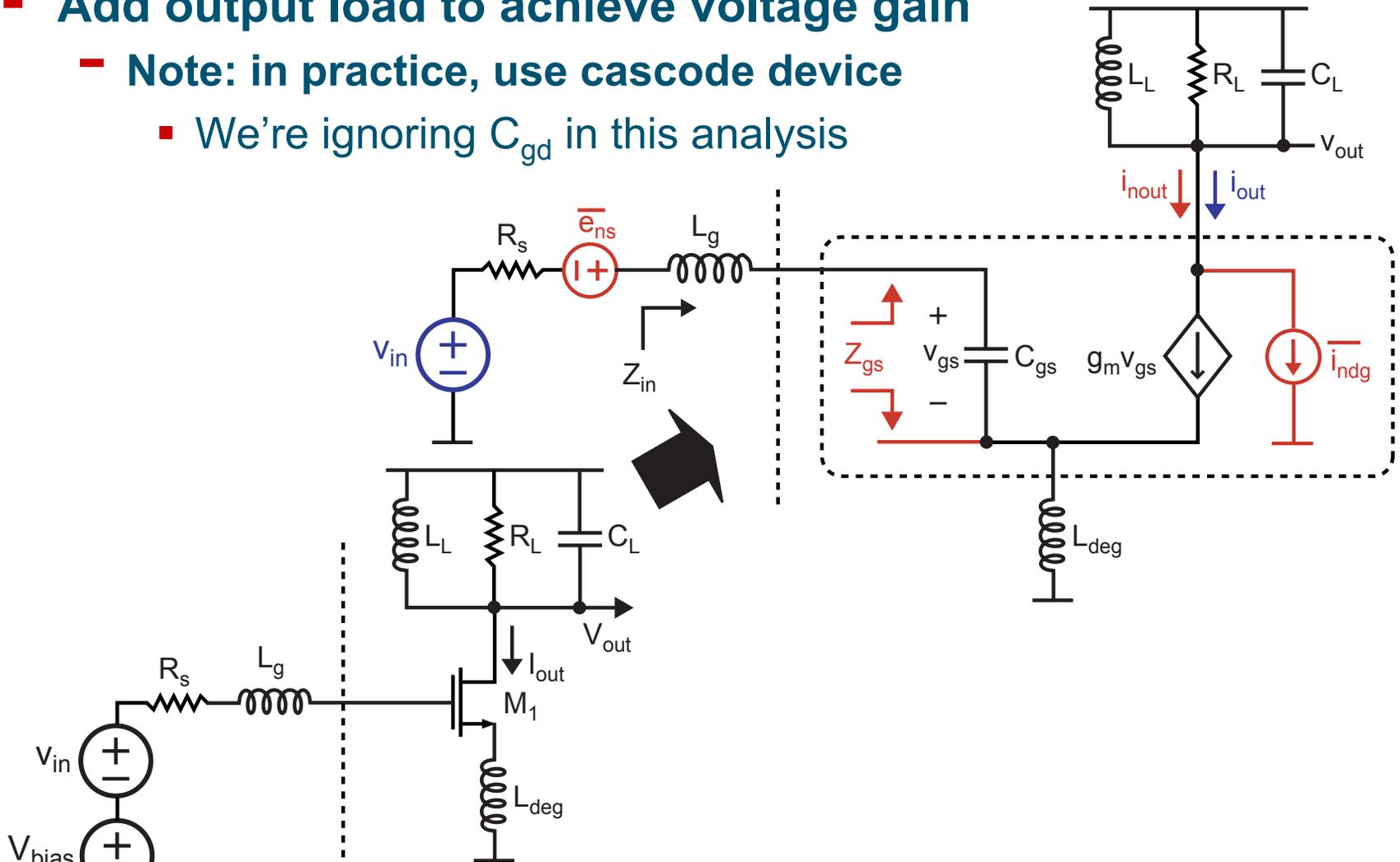
- L_g calculated as

$$\frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = \omega_o \Rightarrow L_g = \frac{1}{\omega_o^2 C_{gs}} - L_{deg}$$

$$\Rightarrow L_g = \frac{1}{(2\pi 1.8e9)^2 147e-15} - 0.19e-9 = 53 \text{ nH}$$

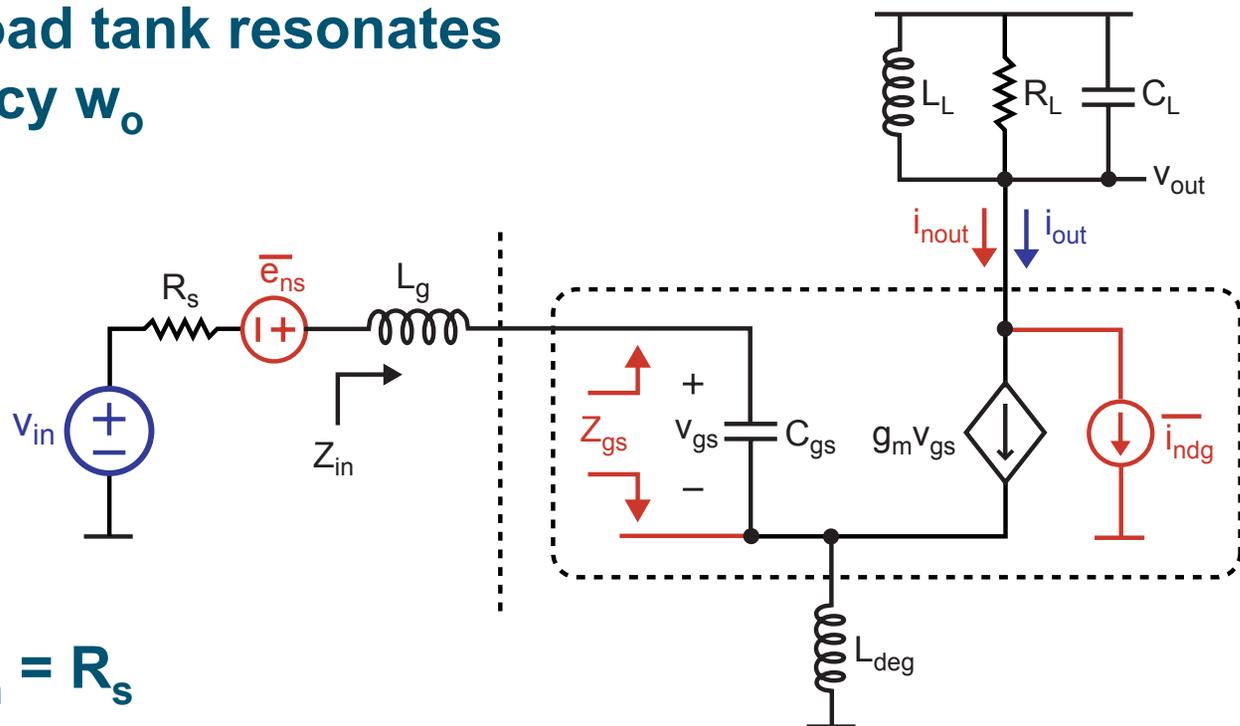
Inclusion of Load (Resonant Tank)

- Add output load to achieve voltage gain
 - Note: in practice, use cascode device
 - We're ignoring C_{gd} in this analysis



Calculation of Gain

- Assume load tank resonates at frequency ω_0



- Assume $Z_{in} = R_s$

$$\Rightarrow v_{gs} = \frac{v_{in}}{2R_s} \left(\frac{1}{j\omega_0 C_{gs}} \right) = \left(\frac{Q}{j} \right) v_{in}$$

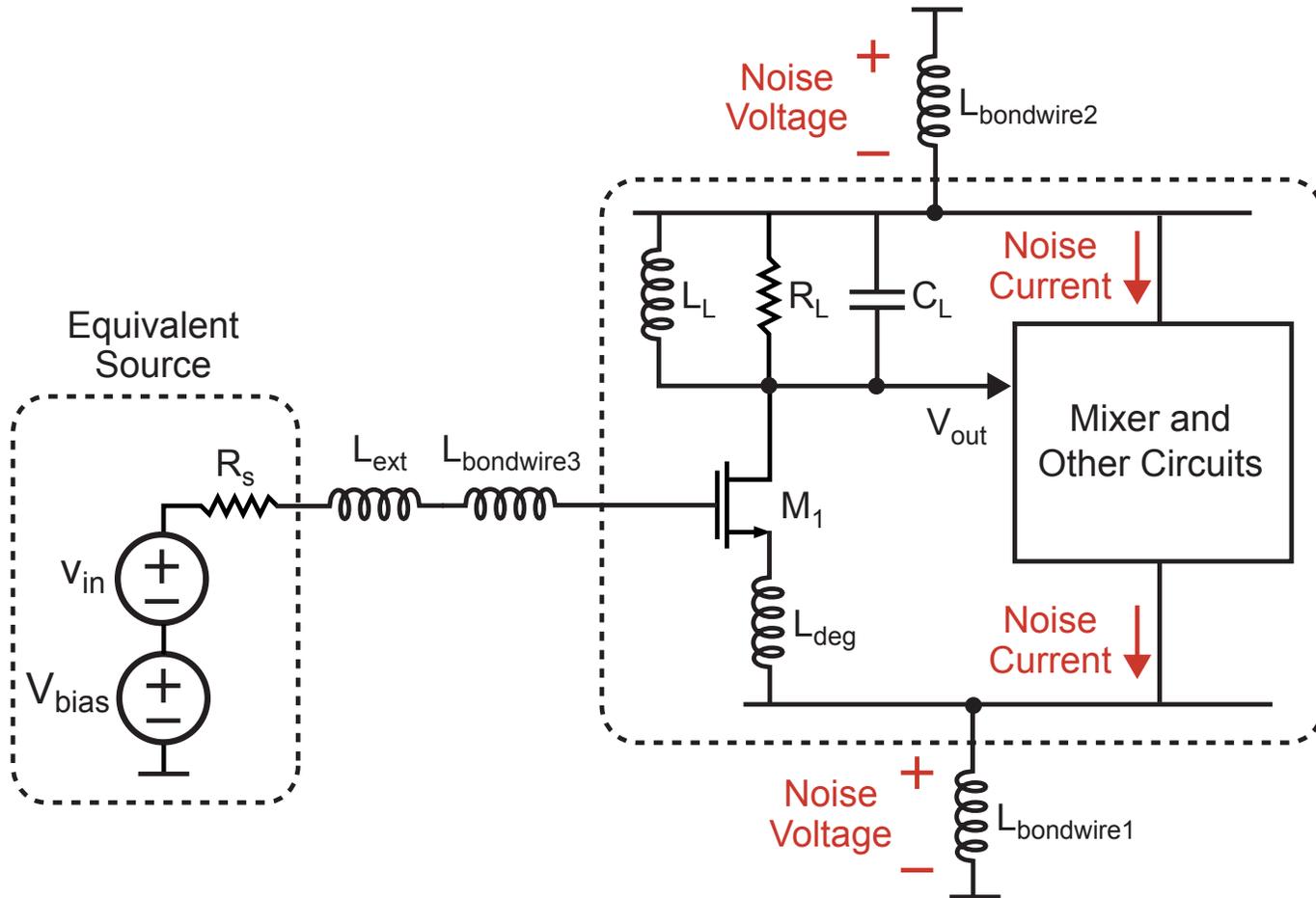
$$\Rightarrow i_{out} = g_m \left(\frac{Q}{j} \right) v_{in} \Rightarrow v_{out} = -g_m R_L \left(\frac{Q}{j} \right) v_{in}$$

Setting of Gain

$$|\text{Gain}| = g_m R_L Q$$

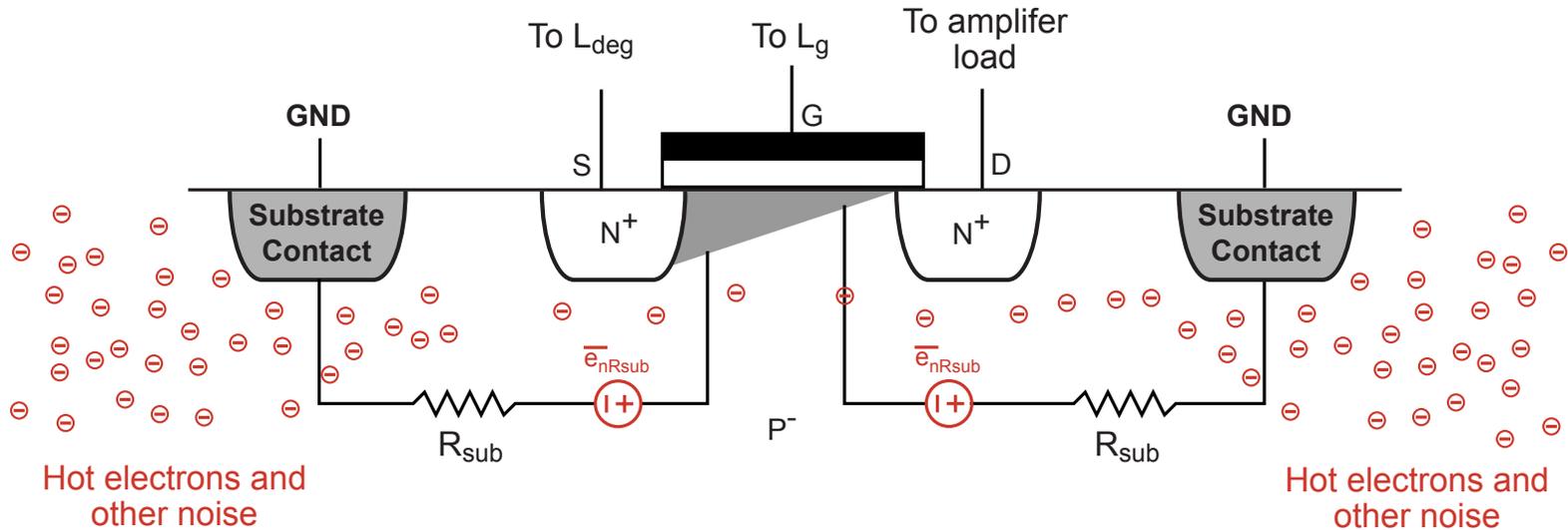
- **Parameters g_m and Q were set by Noise Figure and IIP3 considerations**
 - Note that Q is of the input matching network, not the amplifier load
- **R_L is the free parameter – use it to set the desired gain**
 - Note that higher R_L for a given resonant frequency and capacitive load will increase Q_L (i.e., Q of the amplifier load)
 - There is a tradeoff between amplifier bandwidth and gain
 - **Generally set R_L according to overall receiver noise and IIP3 requirements (higher gain is better for noise)**
 - Very large gain (i.e., high Q_L) is generally avoided to minimize sensitivity to process/temp variations that will shift the center frequency

The Issue of Package Parasitics



- **Bondwire (and package) inductance causes two issues**
 - Value of degeneration inductor is altered
 - Noise from other circuits couples into LNA

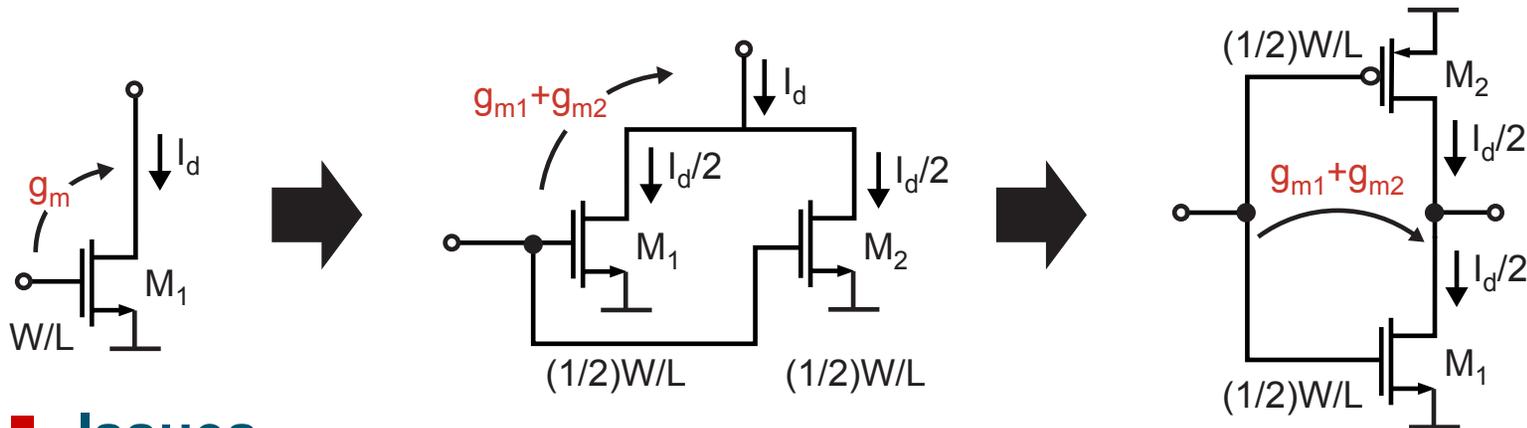
Note: Be Generous with Substrate Contact Placement



- **Having an abundance of nearby substrate contacts helps in three ways**
 - Reduces possibility of latch up issues
 - Lowers R_{sub} and its associated noise
 - Impacts LNA through backgate effect (g_{mb})
 - Absorbs stray electrons from other circuits that will otherwise inject noise into the LNA
- **Negative: takes up a bit extra area**

Another CMOS LNA Topology

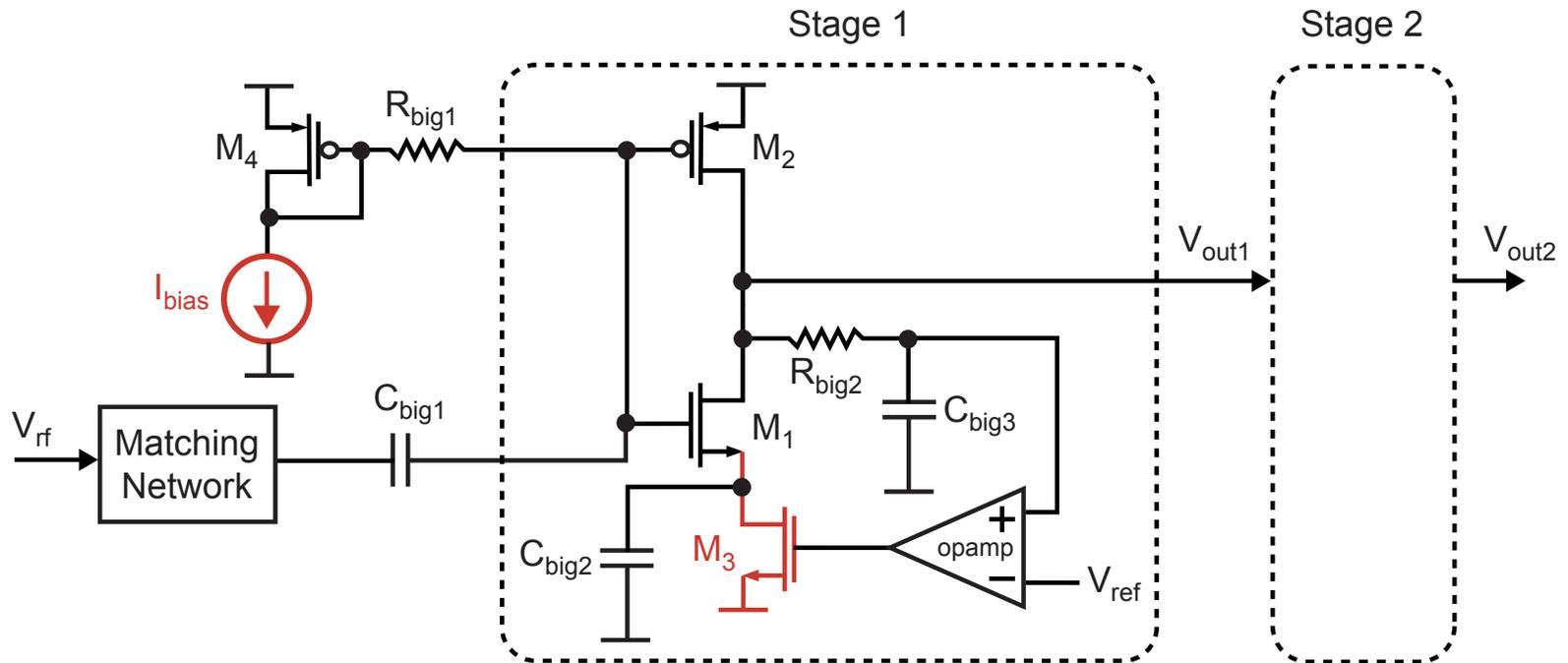
- Consider increasing g_m for a given current by using both PMOS and NMOS devices
 - Key idea: re-use of current



■ Issues

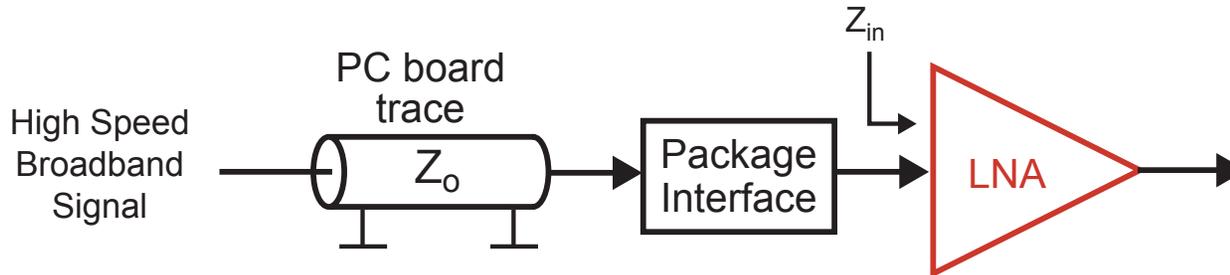
- PMOS device has poorer transconductance than NMOS for a given amount of current, and f_t is lower
- Not completely clear there is an advantage to using this technique, but published results are good
 - See A. Karanicolas, "A 2.7 V 900-MHz CMOS LNA and Mixer", JSSC, Dec 1996

Biasing for LNA Employing Current Re-Use



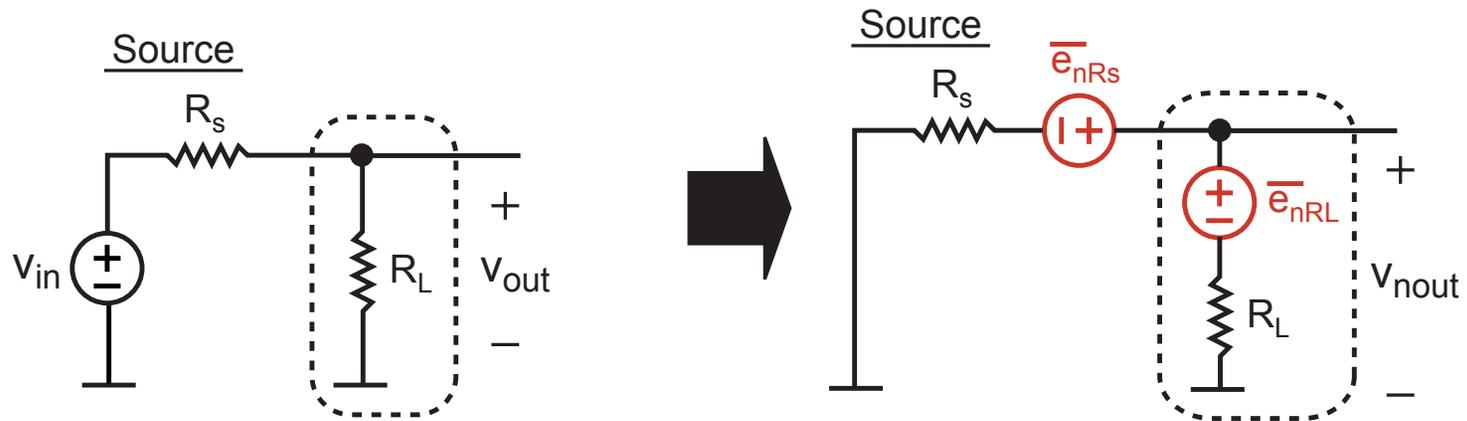
- PMOS is biased using a current mirror
- NMOS current adjusted to match the PMOS current
- Note: not clear how the matching network is achieving a 50 Ohm match
 - Perhaps parasitic bondwire inductance is degenerating the PMOS or NMOS transistors?

Broadband LNA Design



- **Most broadband systems are not as stringent on their noise requirements as wireless counterparts**
- **Equivalent input voltage is often specified rather than a Noise Figure**
- **Typically use a resistor to achieve a broadband match to input source**
 - We know from Lecture 8 that this will limit the noise figure to be higher than 3 dB
- **For those cases where low Noise Figure is important, are there alternative ways to achieve a broadband match?**

Recall Noise Factor Calculation for Resistor Load



- **Total output noise**

$$\overline{v_{nout}^2} = \left(\frac{R_L}{R_s + R_L} \right)^2 \overline{e_{nRs}^2} + \left(\frac{R_s}{R_s + R_L} \right)^2 \overline{e_{nRL}^2}$$

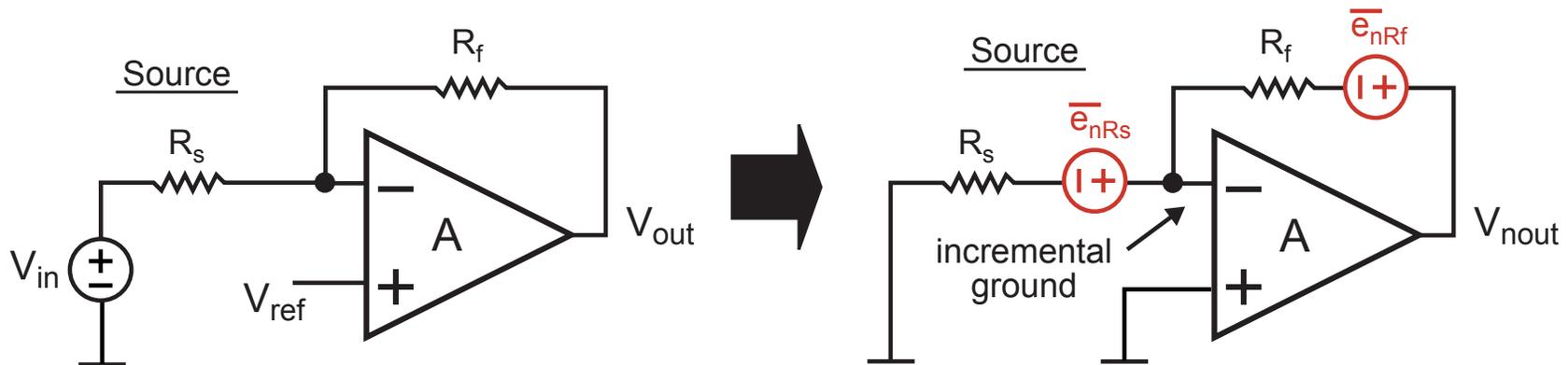
- **Total output noise due to source**

$$\overline{v_{nout}^2} = \left(\frac{R_L}{R_s + R_L} \right)^2 \overline{e_{nRs}^2}$$

- **Noise Factor**

$$F = 1 + \left(\frac{R_s}{R_L} \right)^2 \frac{\overline{e_{nRL}^2}}{\overline{e_{nRs}^2}} = 1 + \left(\frac{R_s}{R_L} \right)^2 \frac{4kTR_L}{4kTR_s} = \boxed{1 + \frac{R_s}{R_L}}$$

Noise Figure For Amp with Resistor in Feedback



- **Total output noise (assume A is large)**

$$\overline{v_{nout}^2} \approx \left(\frac{-R_f}{R_s} \right)^2 \overline{e_{nRs}^2} + \overline{e_{nRf}^2}$$

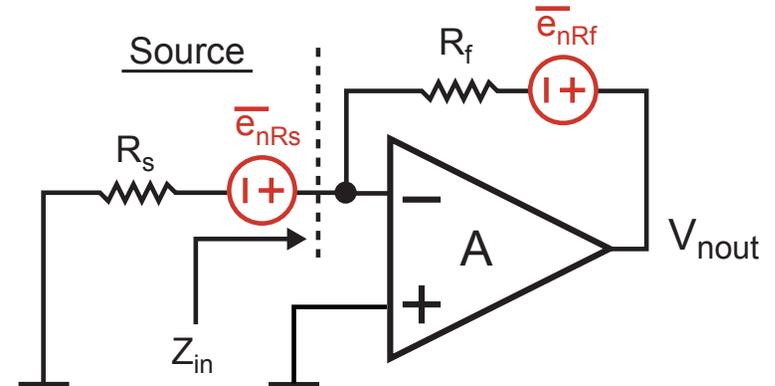
- **Total output noise due to source (assume A is large)**

$$\overline{v_{nout}^2} \approx \left(\frac{-R_f}{R_s} \right)^2 \overline{e_{nRs}^2}$$

- **Noise Factor**

$$F \approx 1 + \left(\frac{R_s}{R_f} \right)^2 \frac{\overline{e_{nRf}^2}}{\overline{e_{nRs}^2}} = 1 + \left(\frac{R_s}{R_f} \right)^2 \frac{4kTR_f}{4kTR_s} = \boxed{1 + \frac{R_s}{R_f}}$$

Input Impedance For Amp with Resistor in Feedback



- Recall from Miller effect discussion that

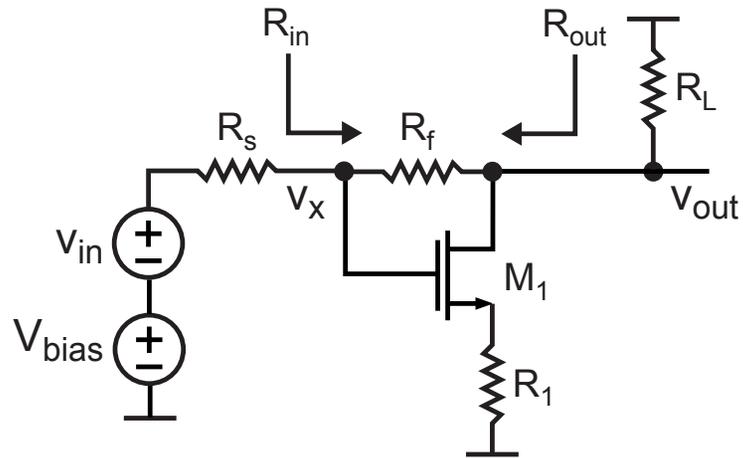
$$Z_{in} = \frac{Z_f}{1 - \text{gain}} = \frac{R_f}{1 + A}$$

- If we choose Z_{in} to match R_s , then

$$R_f = (1 + A)Z_{in} = (1 + A)R_s$$

- Therefore, Noise Figure lowered by being able to choose a large value for R_f since $F \approx 1 + \frac{R_s}{R_f}$

Example – Series-Shunt Amplifier



- Recall that the above amplifier was analyzed in Lecture 5
- Tom Lee points out that this amplifier topology is actually used in noise figure measurement systems such as the Hewlett-Packard 8970A
 - It is likely to be a much higher performance transistor than a CMOS device, though