6.976

High-Speed Communication Circuits and Systems

Lecture 29

Lowpass and Bandpass Delta-Sigma Modulation

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ANALOG
DEVICES

Outline

1 ΔΣ Basics

   1^{st}-Order Modulator

2 Advanced ΔΣ

   High-Order ΔΣ Modulators

   Multi-bit and Multi-Stage Modulation

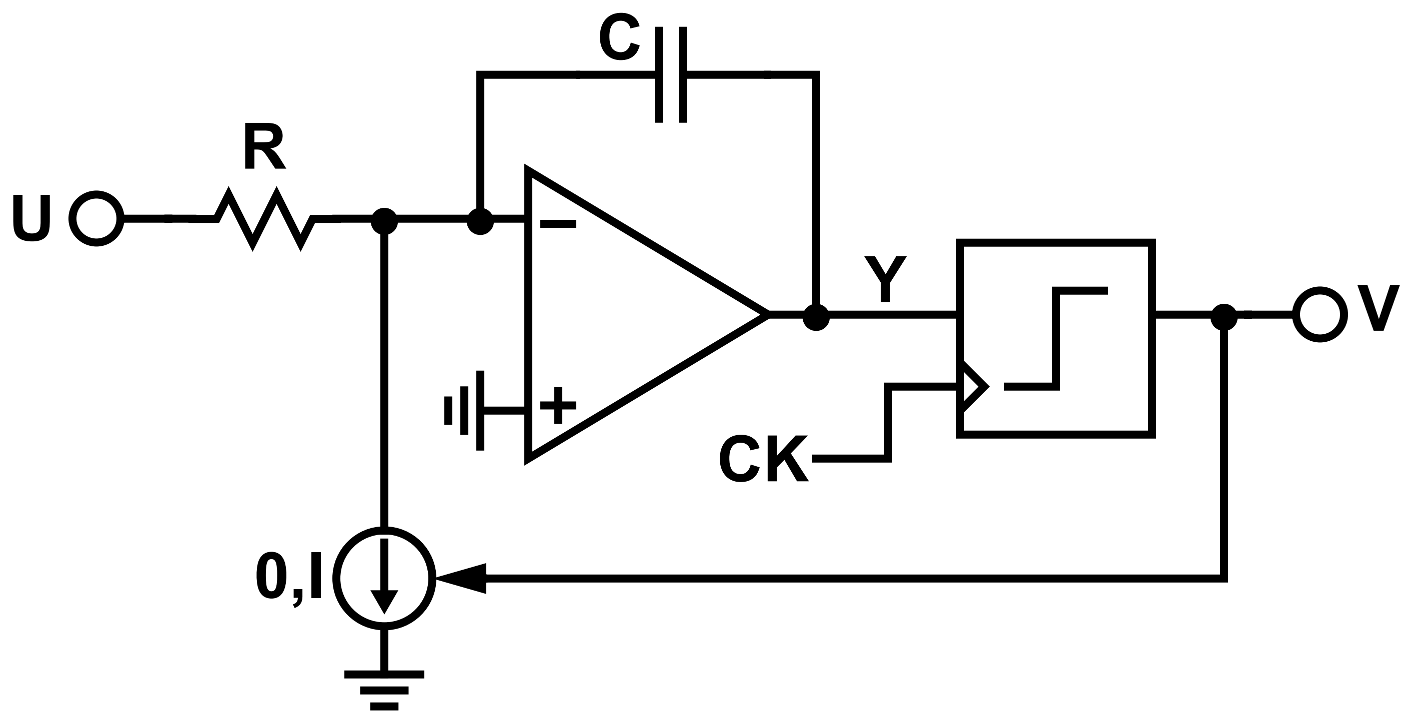
3 Bandpass ΔΣ Modulation

4 Example Bandpass ADC

1. ΔΣ Basics

CTMOD1: A 1st-Order Continuous-Time $\Delta\Sigma$ Modulator

- The input signal, U, is converted into a sequence of bits, V $\in$ (0,1).



Properties of CTMOD1

DC Inputs

- **Integrator ensures that input current is exactly balanced by the (average) feedback current**
  - **"Infinite resolution"**
- **Signals which alias to DC are rejected**
  - **"Inherent anti-aliasing"**

Non-ideal Effects in CTMOD1

- **Component shifts**

  $R \rightarrow R+\Delta R$ or $I \rightarrow I+\Delta I$ merely changes full-scale.

  $C \rightarrow C+\Delta C$ scales the output of the integrator, but does not affect the comparator's decisions.

- **Op-amp offset, input bias current, DAC imbalance**

  All translate into a DC offset, which is unimportant in many communications applications.

- **Comparator offset & hysteresis**

  Overcome by integrator.

- **Finite op-amp gain**

  Creates "dead-bands."

Non-ideal Effects (cont'd)

- **DAC jitter**

  Adds "noise."

- **Resistor nonlinearity (e.g. due to self-heating)**

  Introduces distortion.

- **DAC nonlinearity**

  Introduces distortion and intermodulation of shaped quantization noise.

- **Capacitor nonlinearity**

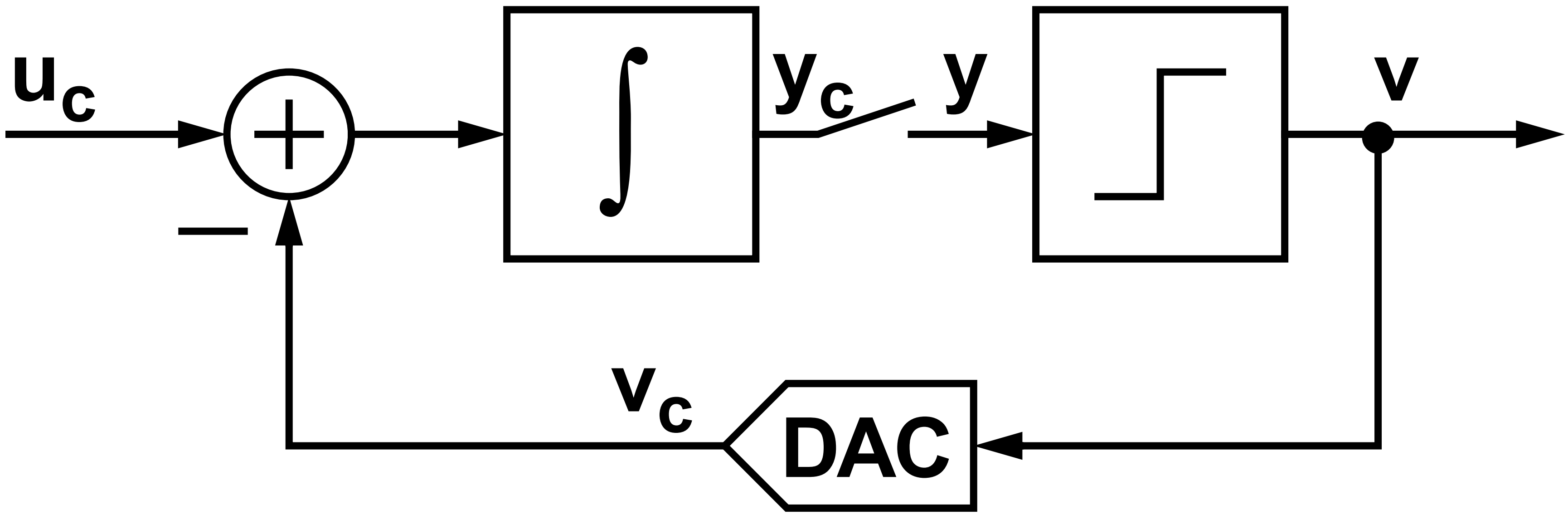
  Irrelevant.

- **Op-amp nonlinearity**

  Same effects as DAC nonlinearity, but less severe.

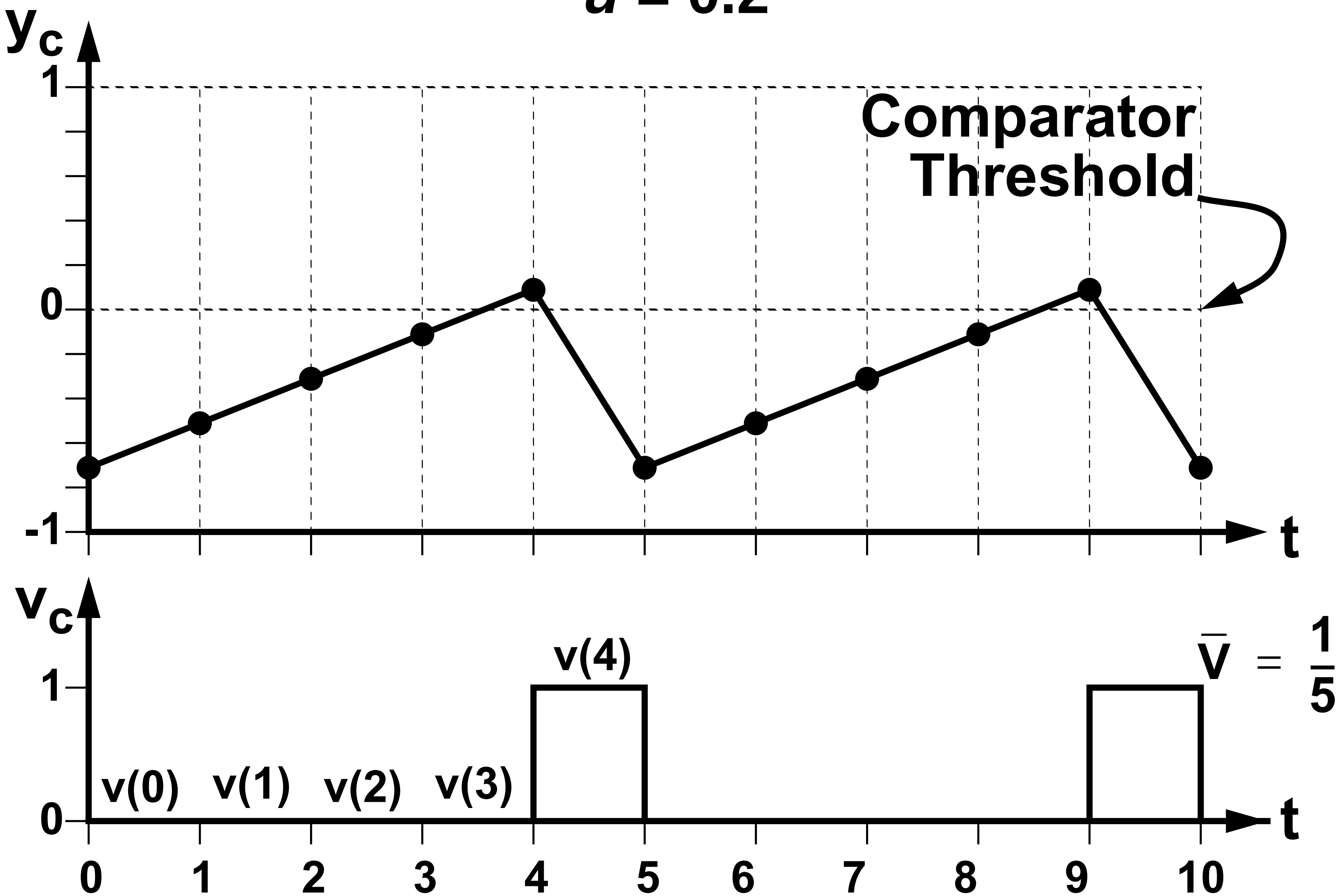
CTMOD1 Model

- **Normalize R=1Ω, C=1F, I=1A, F_s=1Hz**
  Full-scale range is [0,1]V.
- **Assume comparator and DAC are delay-free**

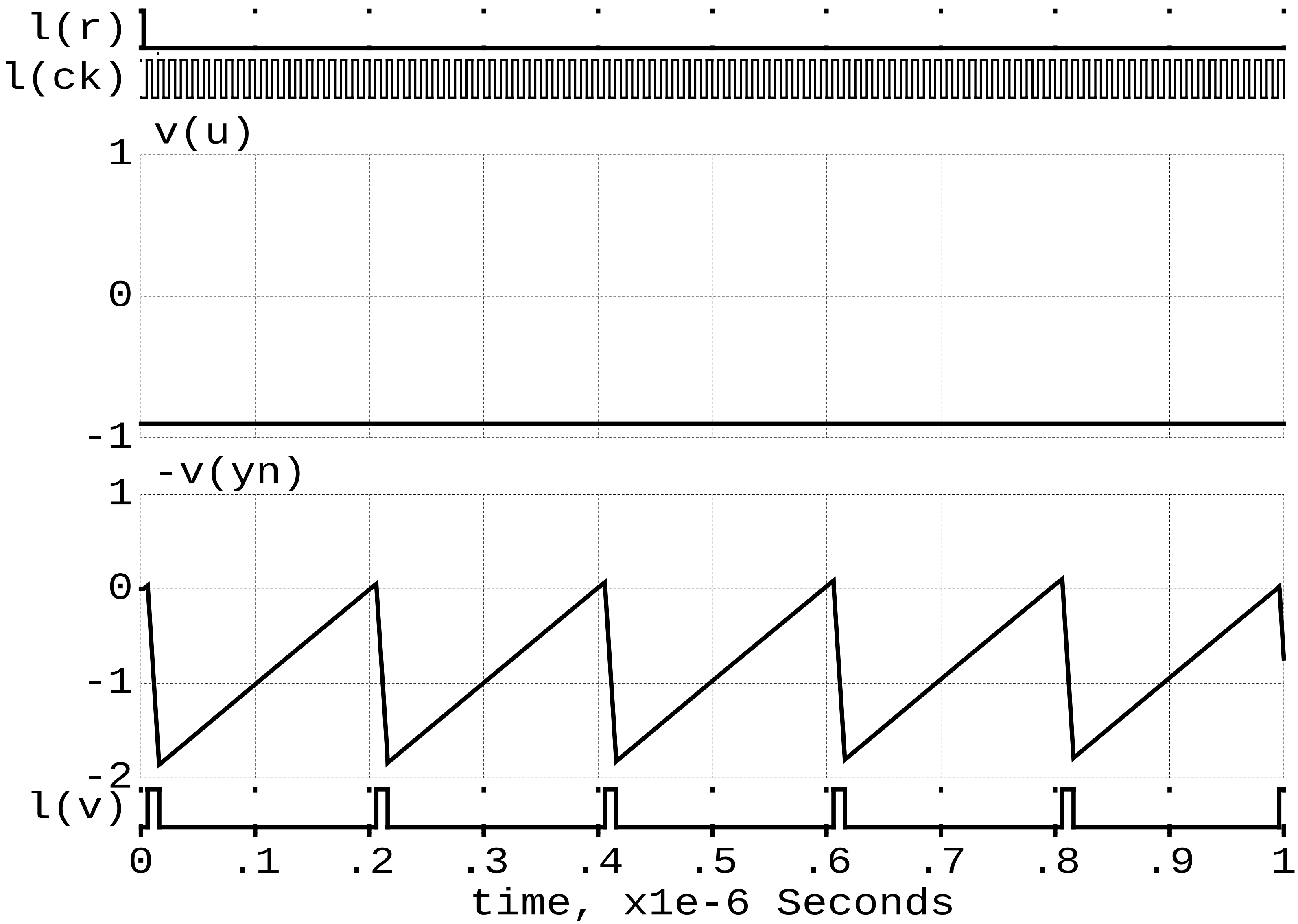


Waveforms/Timing

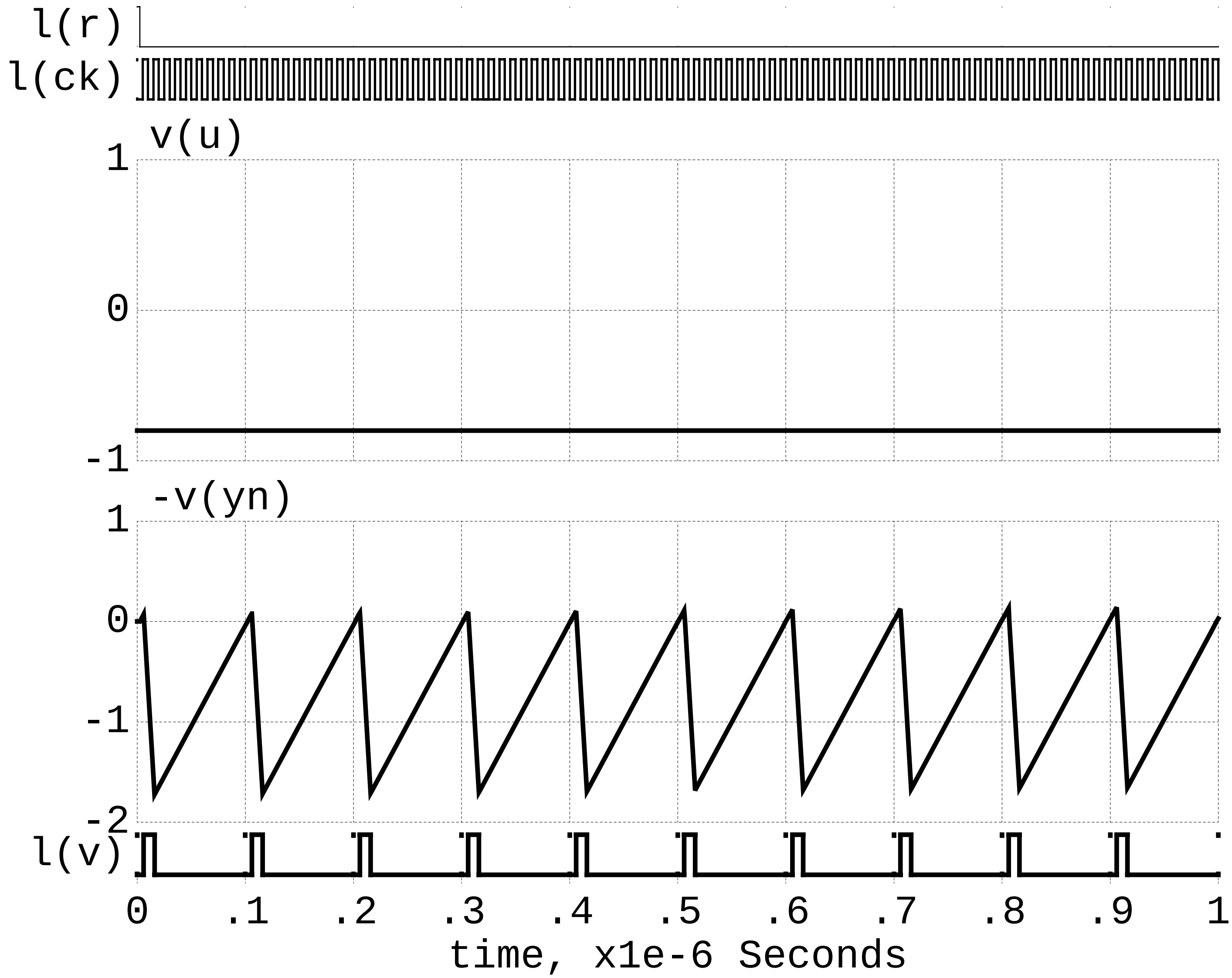
$u = 0.2$



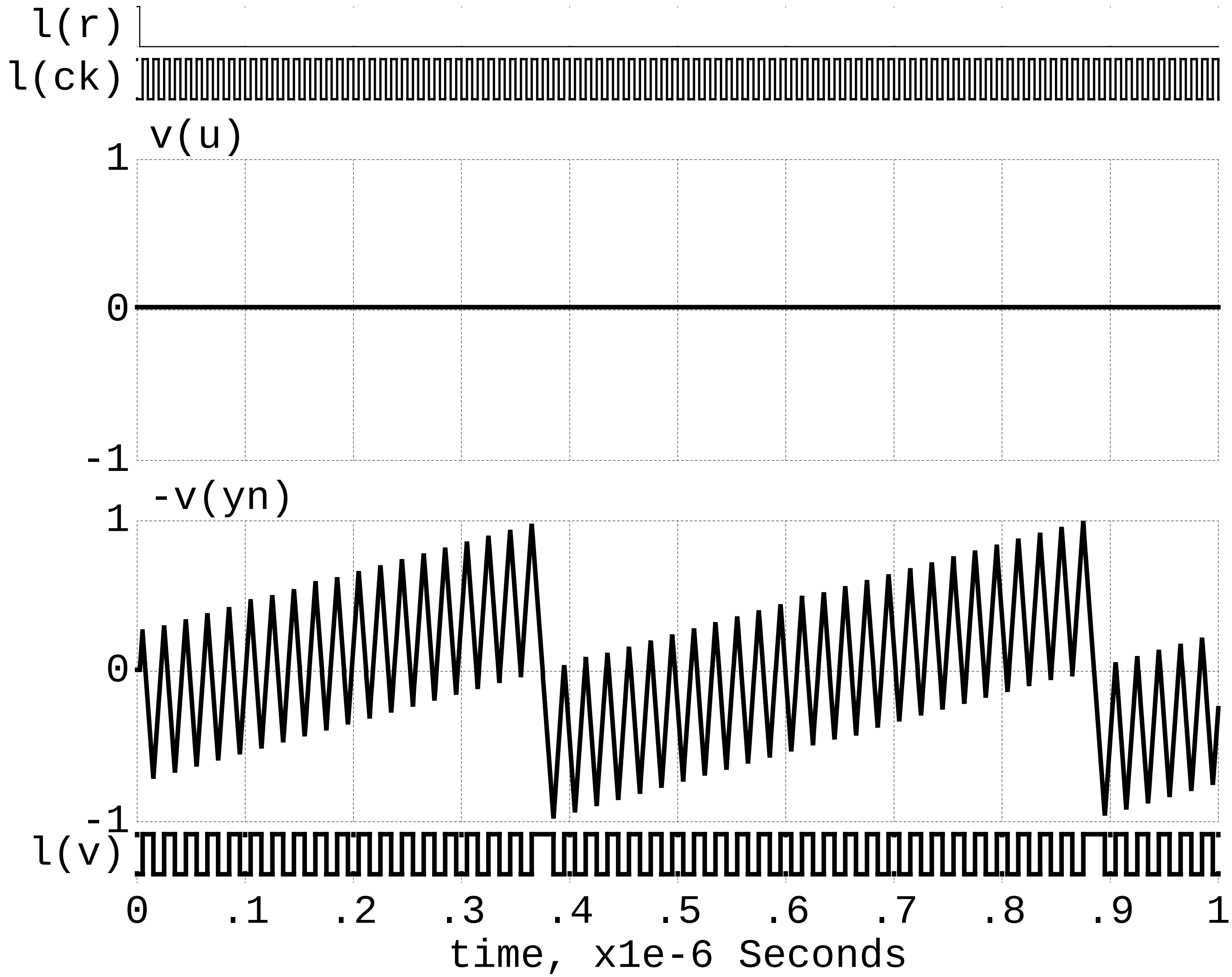
CTMOD1 @ 5% 1's density



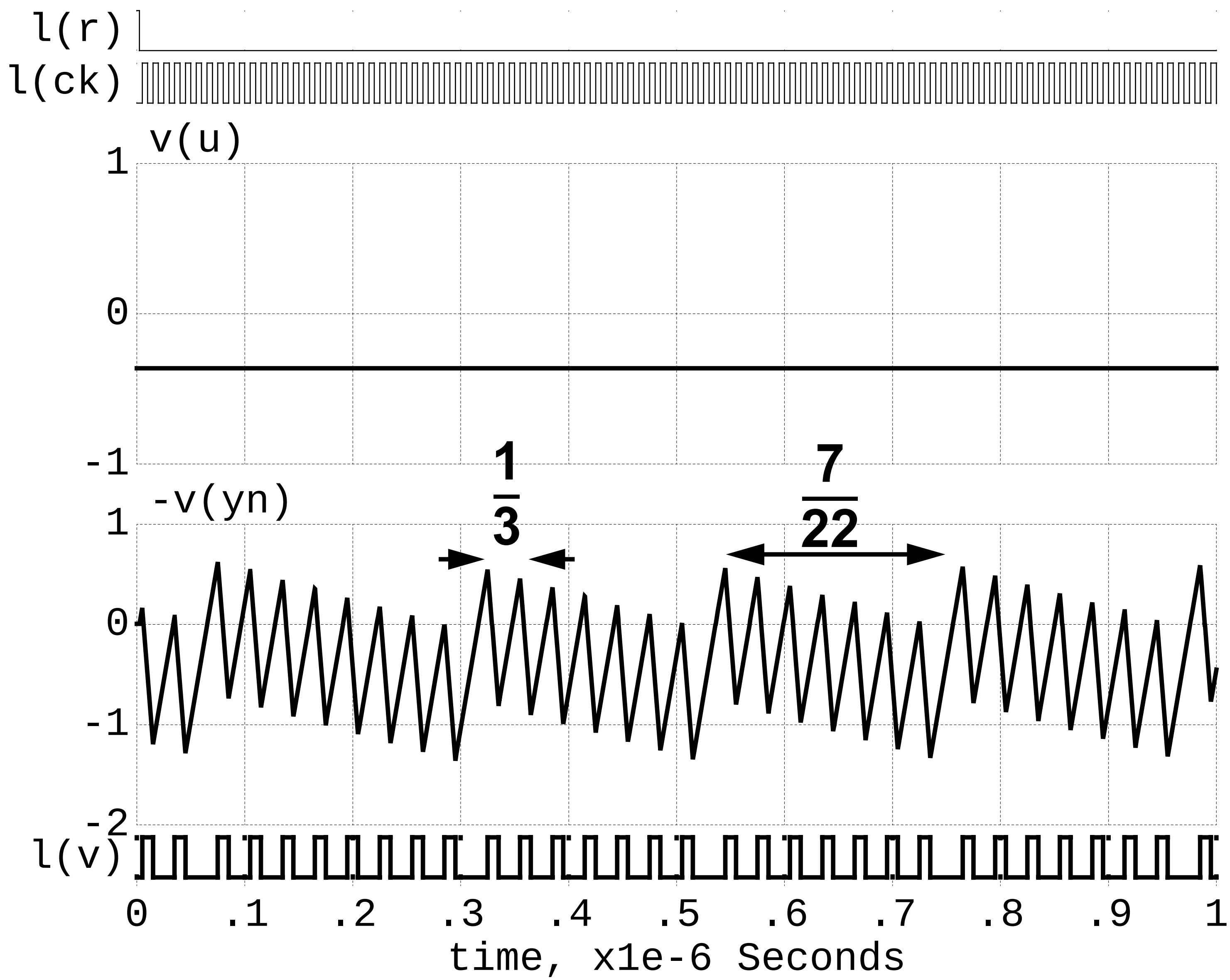
CTMOD1 @ 10% 1's density



CTMOD1 @ 51% 1's density



CTMOD1 @1/π 1's density



Analysis of CTMOD1

From the diagram:

$$y_c(n) = y_c(n-1) + \int_{n-1}^{n} (u_c(\tau) - v_c(\tau))\, d\tau$$

1) Sample y_c at integer time and identify $y(n) = y_c(n)$.

2) Observe that $\int_{n-1}^{n} v_c(\tau)\, d\tau = v(n-1)$

3) Define $u(n) = \int_{n-1}^{n} u_c(\tau)\, d\tau$

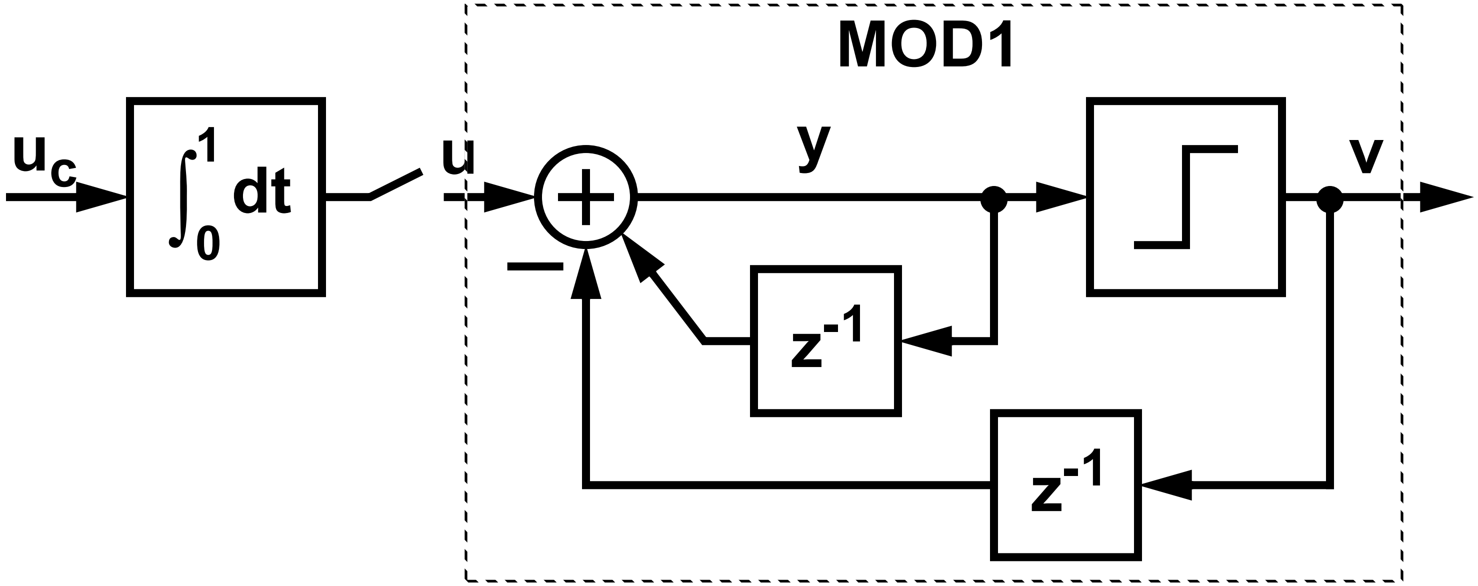
THEN

$$y(n) = y(n-1) + u(n) - v(n-1)$$

Also, from the diagram

$$v(n) = Q(y(n))$$

CTMOD1 Equivalent

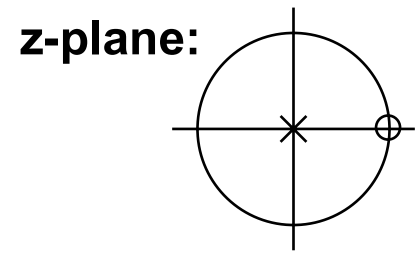


- CTMOD1 is the same as a discrete-time first-order modulator (MOD1) preceded by a sinc filter!

CTMOD1 NTF and STF

- **The NTF is the same as MOD1:**

$$\mathrm{NTF}(z) = 1 - z^{-1}$$

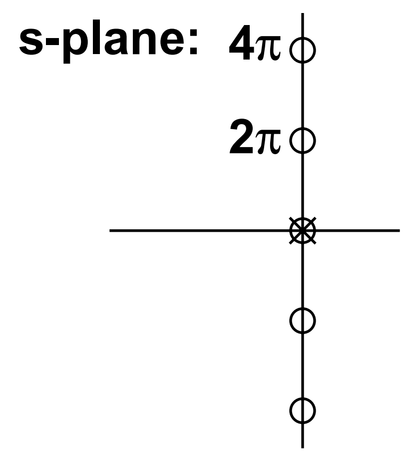


- **MOD1's STF is 1, so the overall STF is just the TF of the prefilter:**

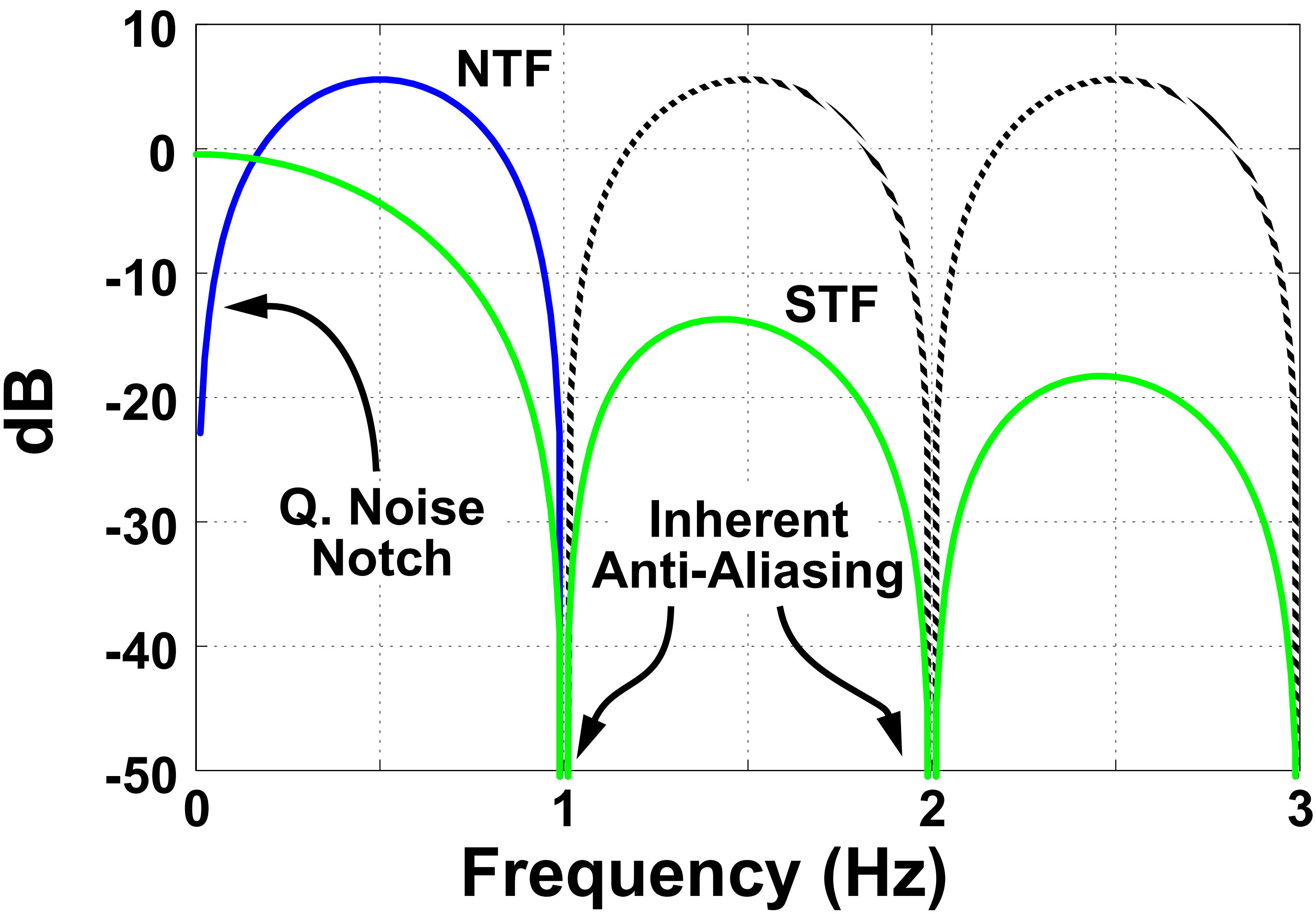
$$\mathrm{STF}(s) = \int_0^{\infty} e^{-st} g_p(t)\,dt$$

$$= \int_0^{1} e^{-st}\,dt = \frac{(1 - e^{-s})}{s}$$

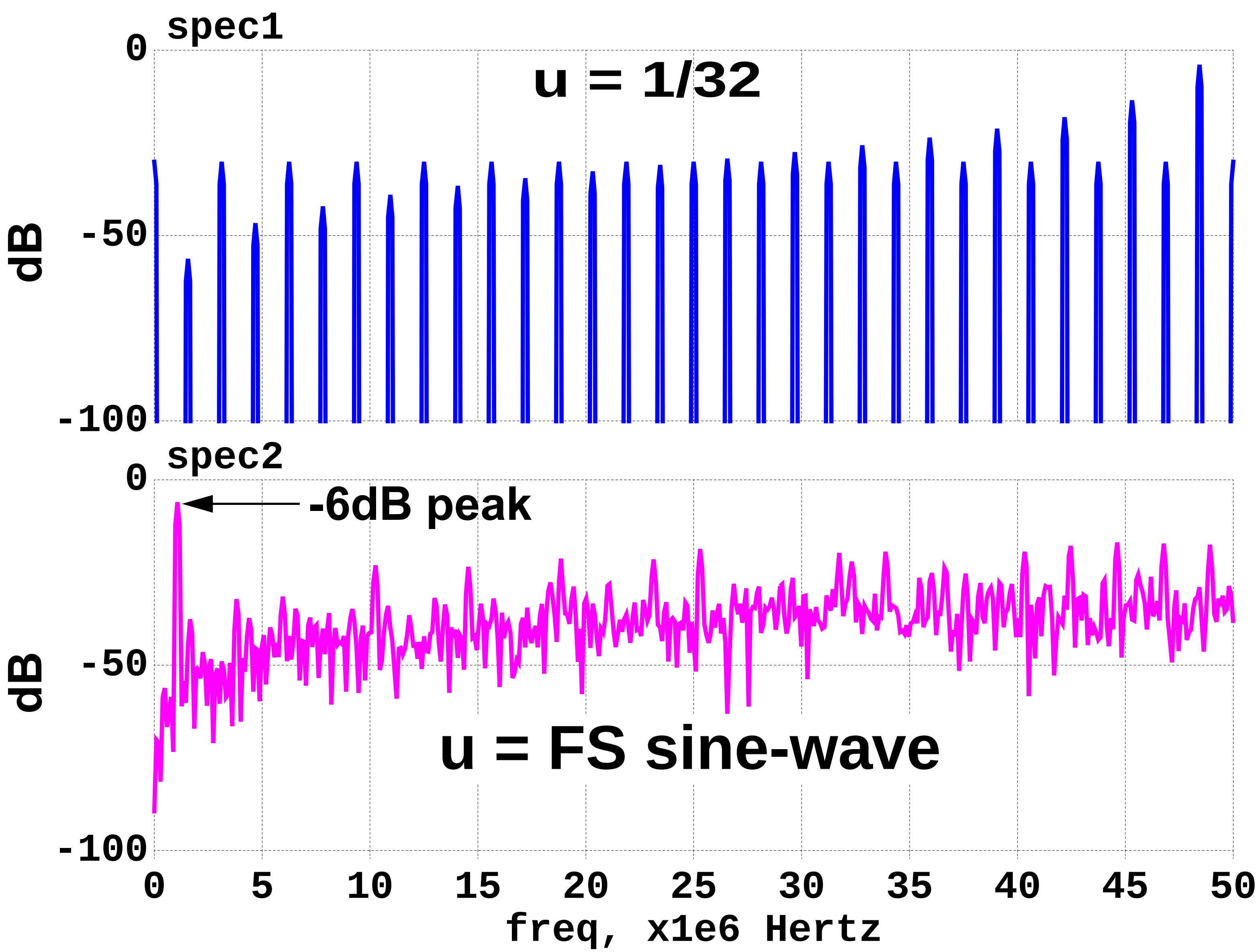
$$= \frac{(1 - z^{-1})}{s}, \text{ where } z = e^{s}$$



Frequency Responses



CTMOD1 Spectra



Properties of MOD1

- **Single-bit quantization yields "inherent linearity."**

  The DAC defines two points and two points can always be joined with a line. (Not so simple in continuous-time.)

- $0 \le u \le 1 \Rightarrow |y| \le 1$

  MOD1 is stable for inputs all the way up to full-scale. The quantizer in MOD1 does not "overload."

- **Assuming the quantization error is white with power σ_e^2, the in-band noise power is**

  $N_0^2 \cong \dfrac{\pi^2 \sigma_e^2}{3(OSR)^3}$. **~12-bit performance at OSR=256.**

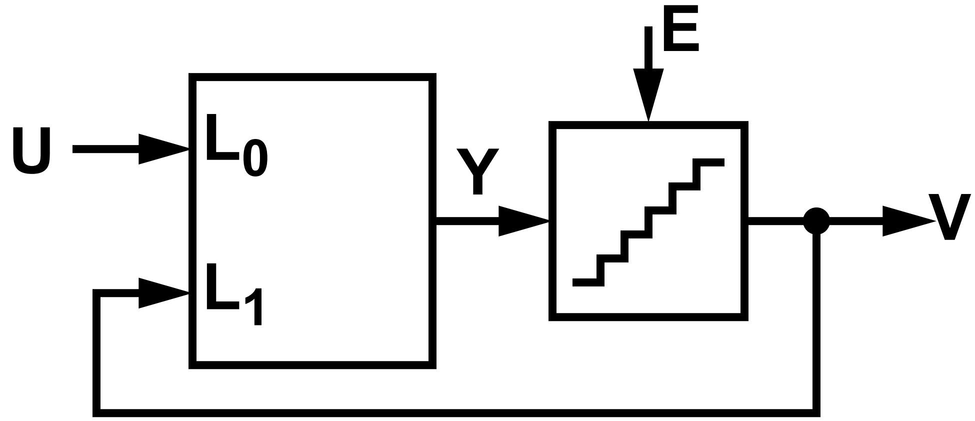
  Doubling OSR reduces noise power by a factor of 8. "1.5 bits increase in SNR per octave increase in OSR"

MOD1 Properties (cont'd)

- **DC input $u = \frac{a}{b}$ results in period-*b* behavior.**
  The spectrum of the error is not white! Spectrum consists of a finite set of harmonics of f_s / b.
- **Irrational DC inputs result in aperiodic behavior.**
  Nonetheless, the spectrum of the error is still discrete!
  Spectrum consists of an infinite number of tones with frequencies that are irrational fractions of f_s.
- **Finite op-amp gain shifts NTF zero inside the unit circle and allows a range of *u* values to produce the same limit cycle.**
  Worst case is around $u = 0, 1, \frac{1}{2}$ etc.;
  yields "dead bands."
- **The behavior of MOD1 is erratic.**

2. Advanced ΔΣ

A Single-Loop ΔΣ Modulator



$$Y = L_0U + L_1V$$
$$V = Y + E$$

$$\Rightarrow$$

$$V = GU + HE\text{, where}$$
$$H = \frac{1}{1 - L_1} \; \& \; G = L_0H$$

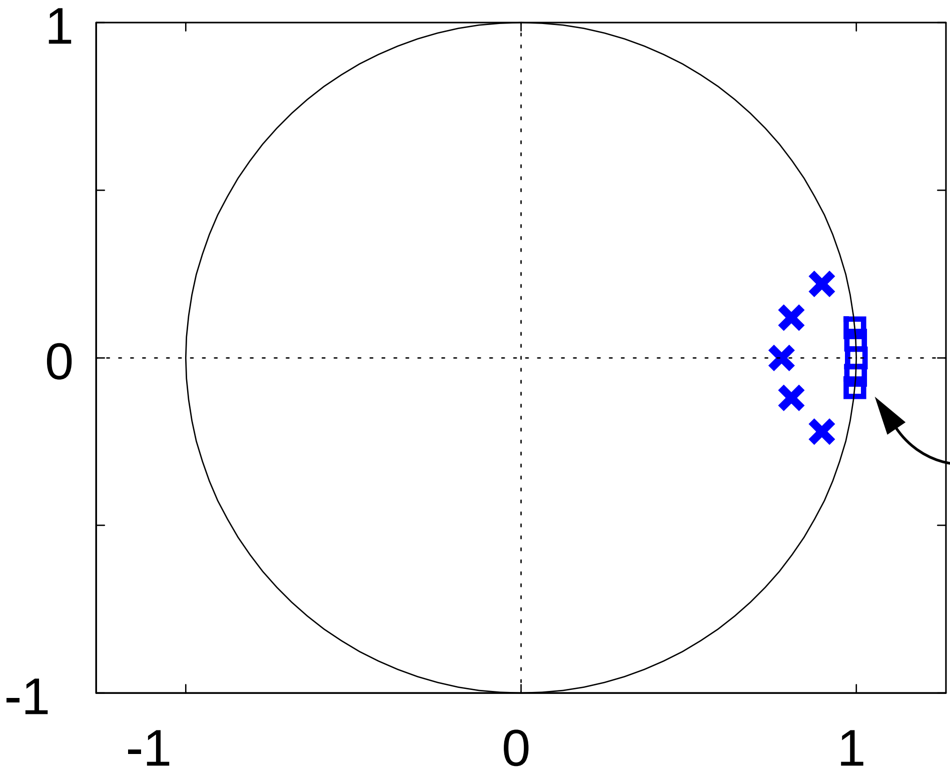
Inverse Relations:

$L_1 = 1 - 1/H$, $L_0 = G/H$

- **The zeros in *H* come from the poles in L_1**

A 5th-Order Lowpass NTF
Zeros optimized for OSR=32

- **Pole/Zero diagram:**

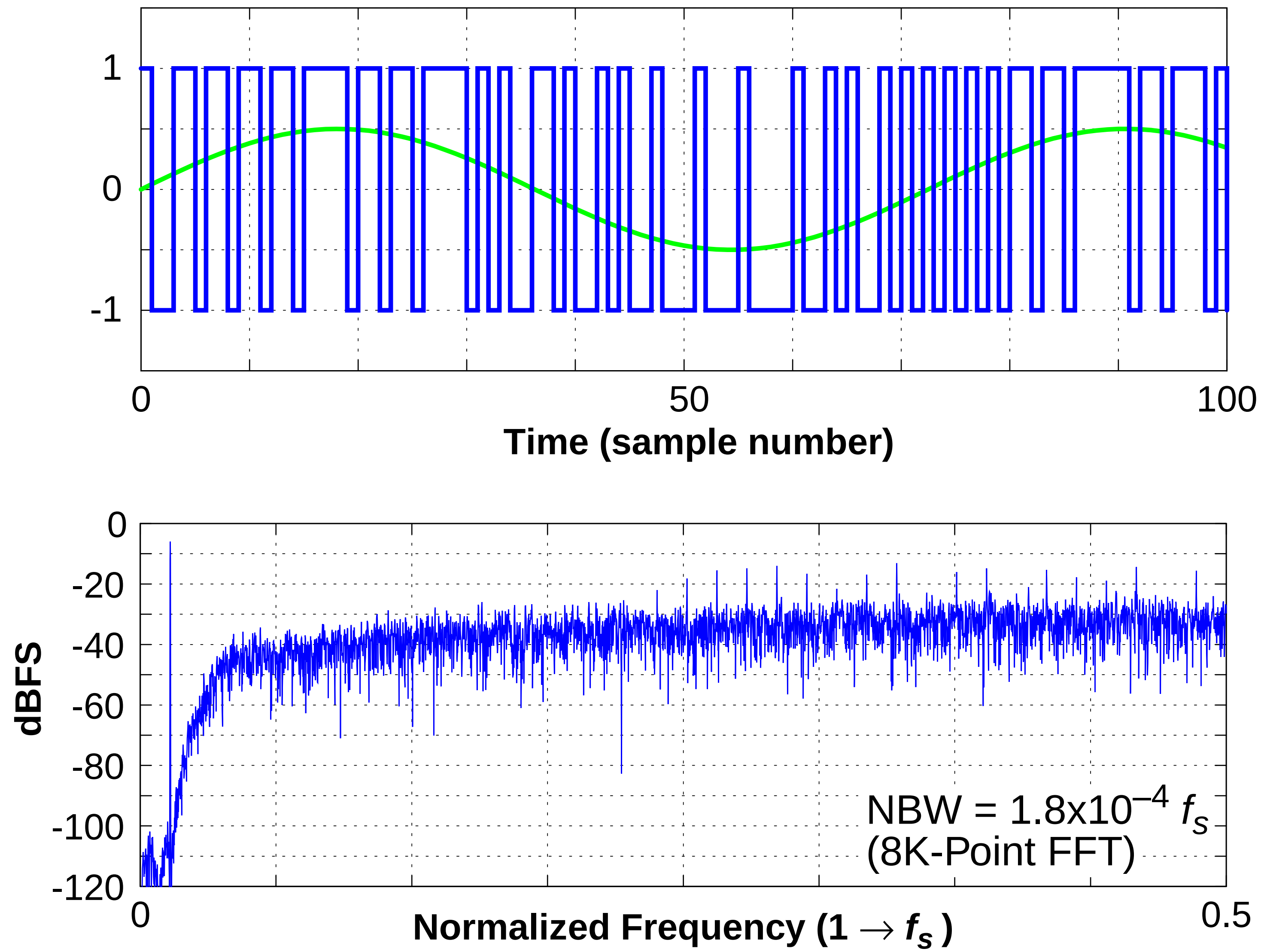


optimization flag

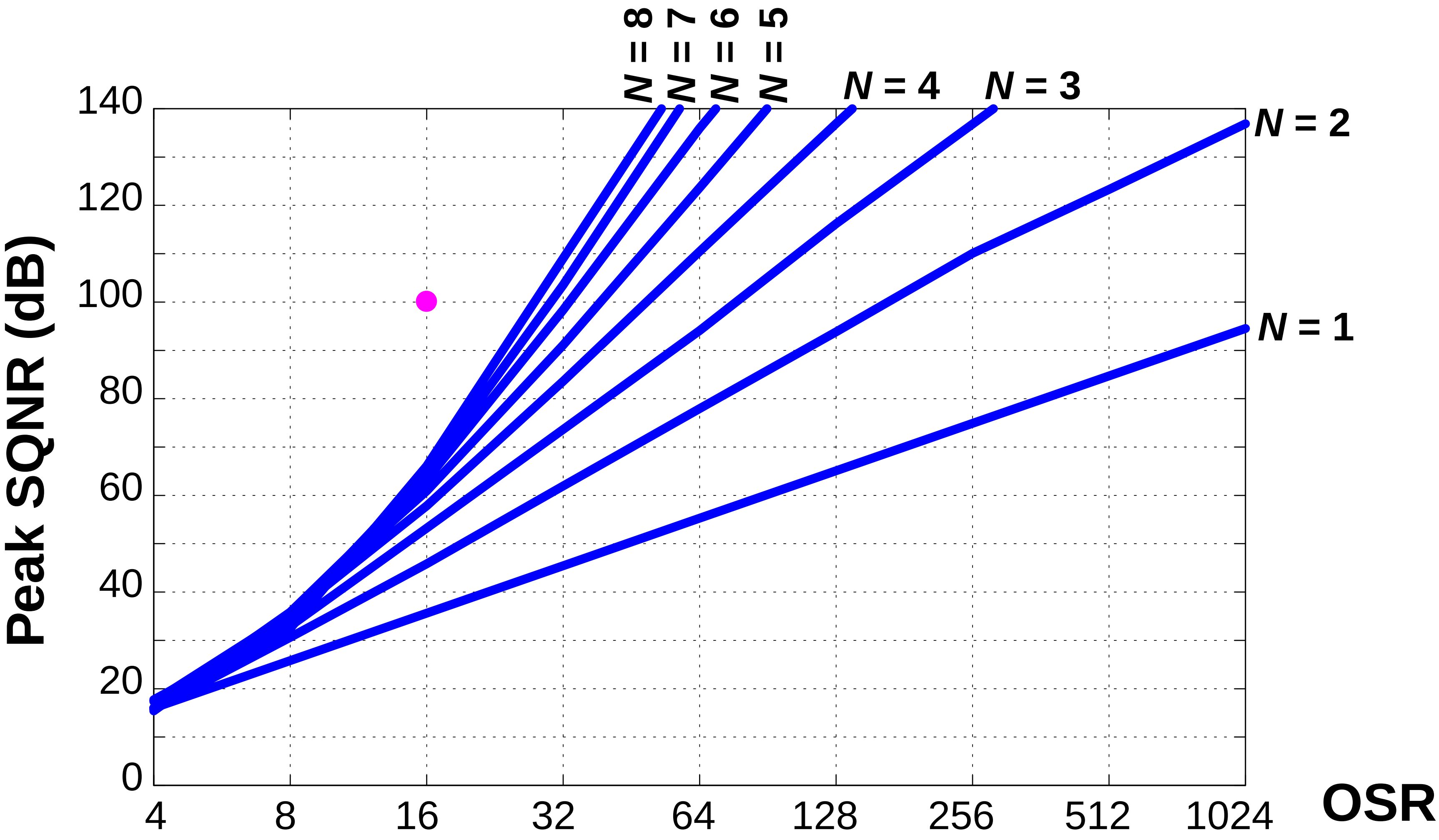
```
OSR = 32;
H = synthesizeNTF(5,OSR,1);
...
```

Zeros spread across the band-of-interest to minimize the rms value of the NTF.
Poles such that ||H|| = 1.5.

Example: 5^{th}-Order Modulator



SQNR Limits for Binary Modulators



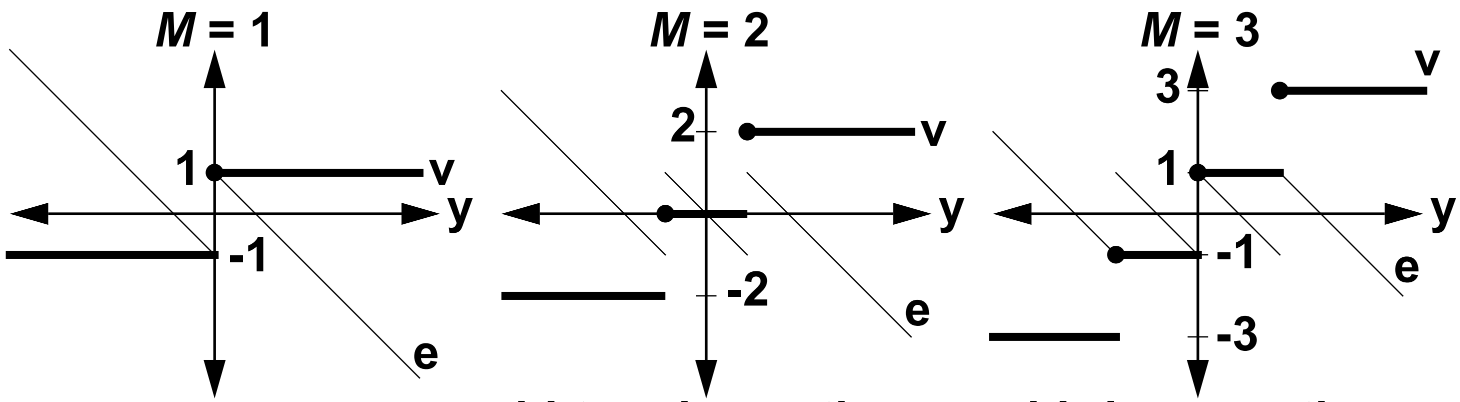
Multi-Bit Quantization

Toolbox Conventions

- **Single-bit quantizer output interpreted as ±1 instead of 0,1.**

  Quantizer step size, Δ, is 2; input range is [-1,+1].

- **Convention for multi-bit quantization is:**

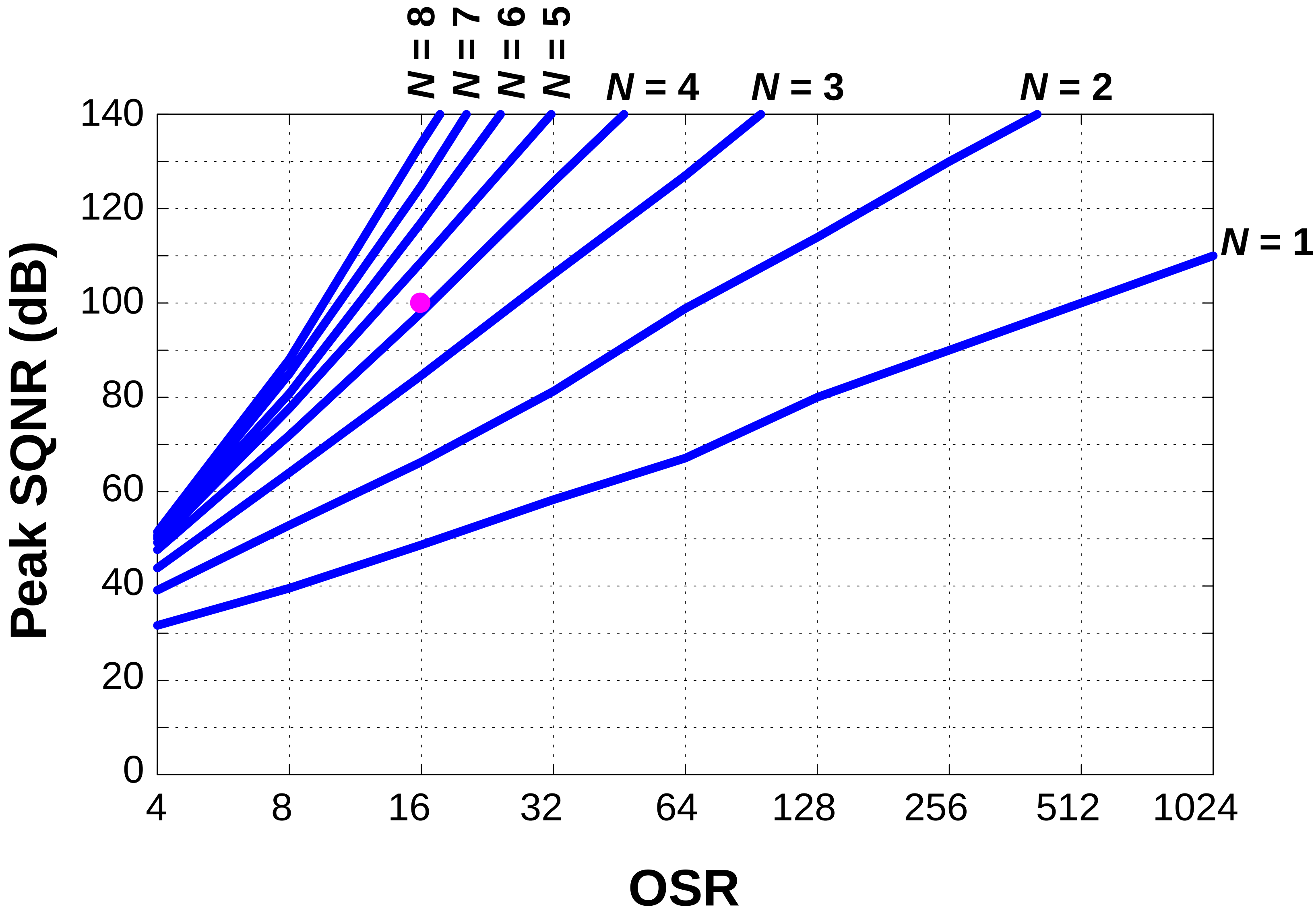


mid-tread quantizer; v: even integers

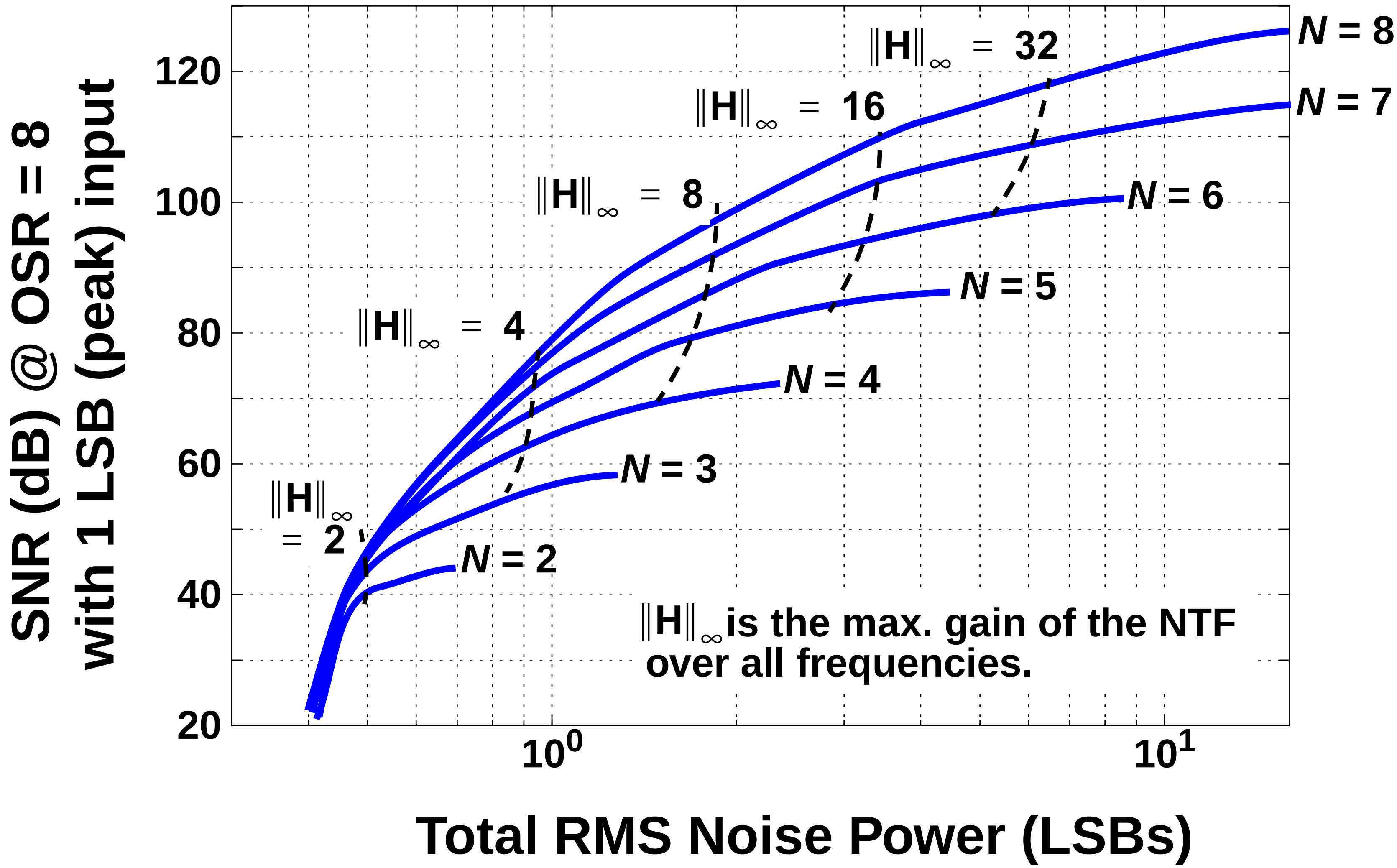
mid-rise quantizer; v: odd integers

Δ = 2; # of Q. levels is *nlev* = *M*+1, from –*M* to +*M*; no-overload range (|e| ≤ 1) is –*nlev* to +*nlev*.

SQNR Limits for 3-bit Modulators



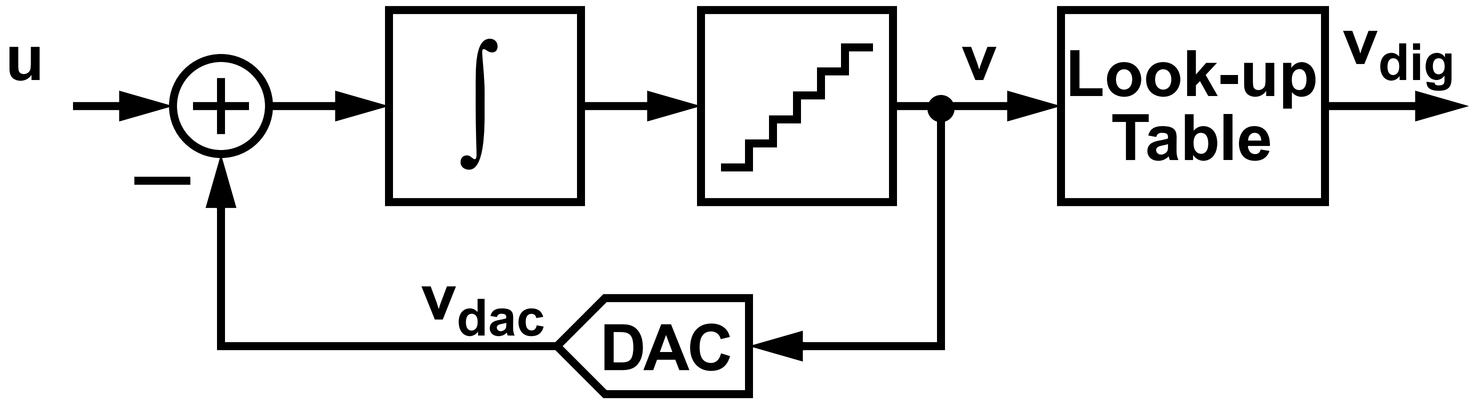
Theoretical SNR Limits for Multi-Bit Modulators



Multi-Bit Quantization
Pros and Cons

- **Multi-bit quantization overcomes stability-induced restrictions on the NTF**
  - Dramatic improvements are possible!
- **Multi-bit quantization loses the inherent linearity property of a binary DAC**
  - DAC levels are not evenly spaced and so cannot be joined with a straight line.
  - DAC errors are effectively added to the input, and thus are not shaped.
  - Can be overcome with calibration, digital correction or mismatch-shaping.

Digital Correction



- **Lookup table contains the digital equivalent of each DAC level**

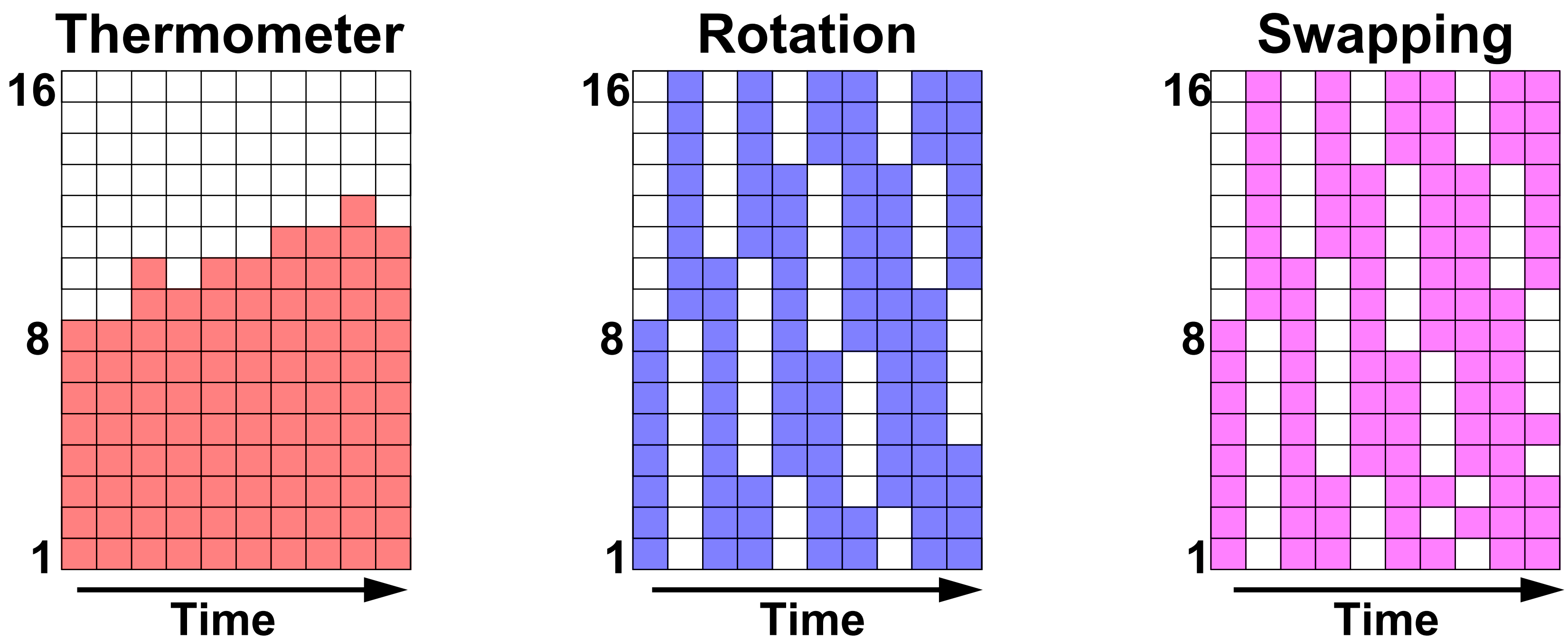
  In practice, the look-up table only needs to store the differences between the actual and ideal DAC levels.

- **Thus $v_{dig} = v_{dac}$, so DAC errors are now shaped by the loop!**

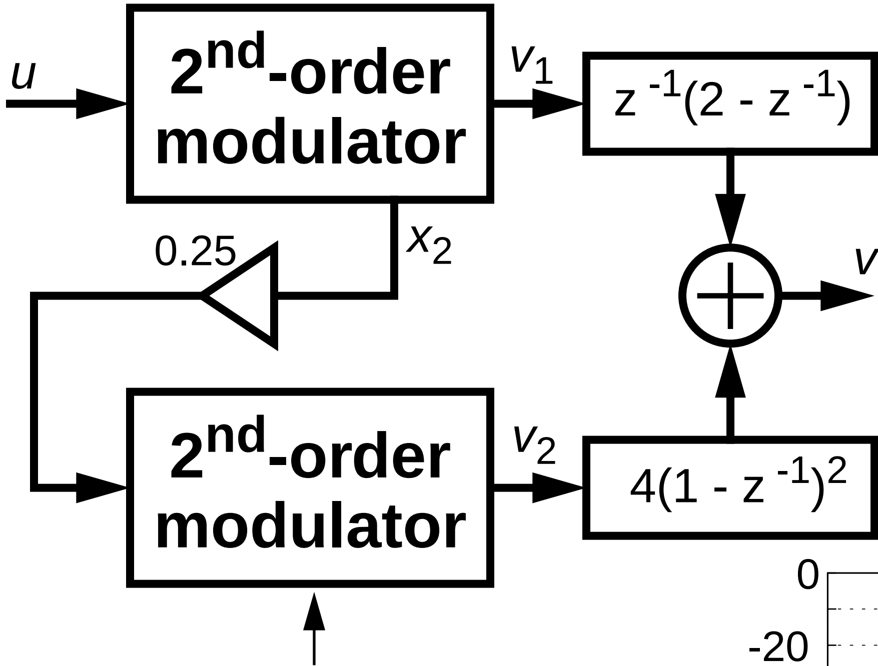
Mismatch-Shaping

- **Shapes mismatch-induced noise by ensuring that each element in a unit-element DAC is driven by a shaped sequence**

  Two popular forms of mismatch-shaping are *element-rotation* and *element-swapping*.

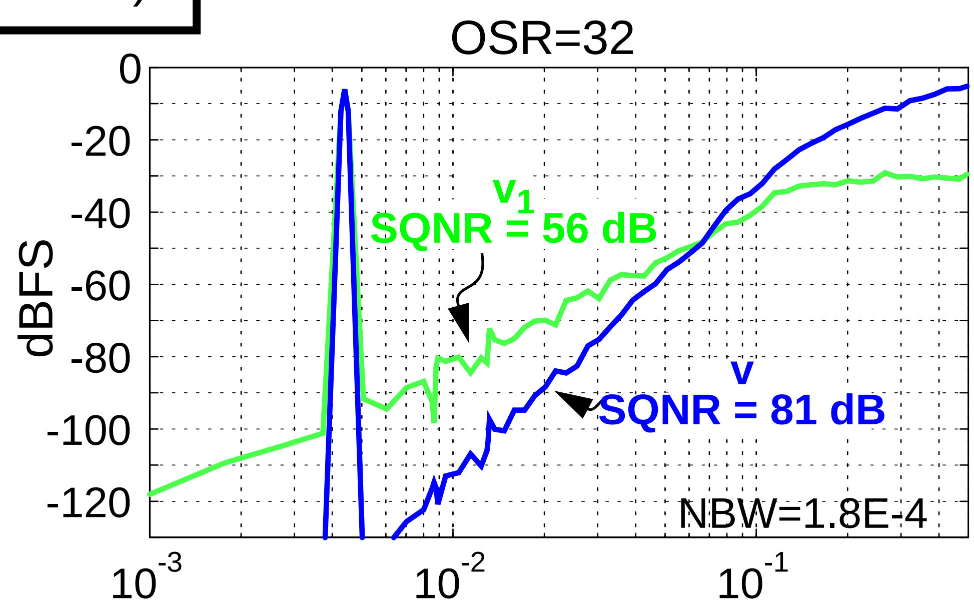


Multi-Stage Modulation



$G = z^{-1}$,
$H = (1 - z^{-1})^2$

```
mod = mod2;
ABCD = mod.ABCD;
[v1 x] = simulateDSM(input,ABCD);
v2 = simulateDSM(x(2,:)/4,ABCD);
v = filter([0 2 -1],1,v1) + ...
  4*filter([1 -2 1],1,v2);
```

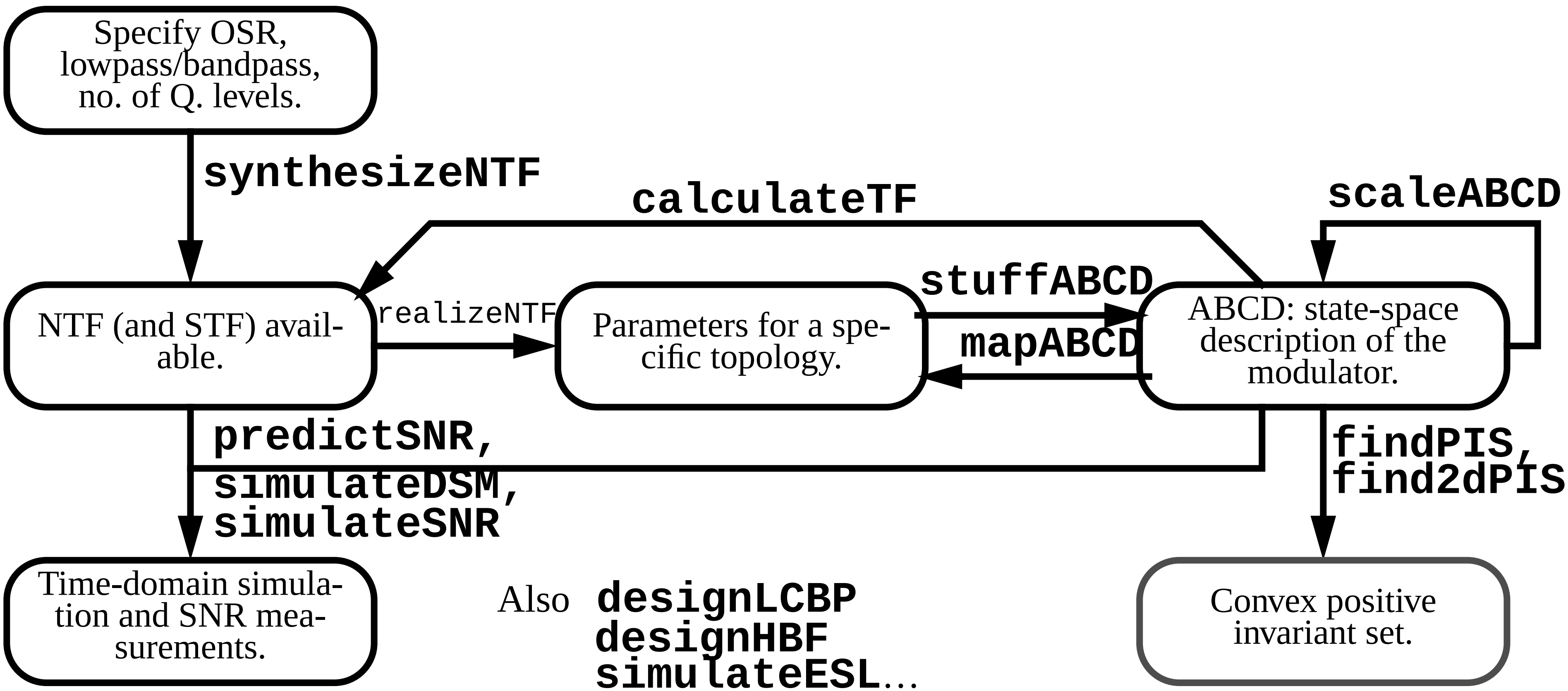


Composite NTF is $4H^2$

ΔΣ Toolbox Summary

http://www.mathworks.com/matlabcentral/fileexchange/

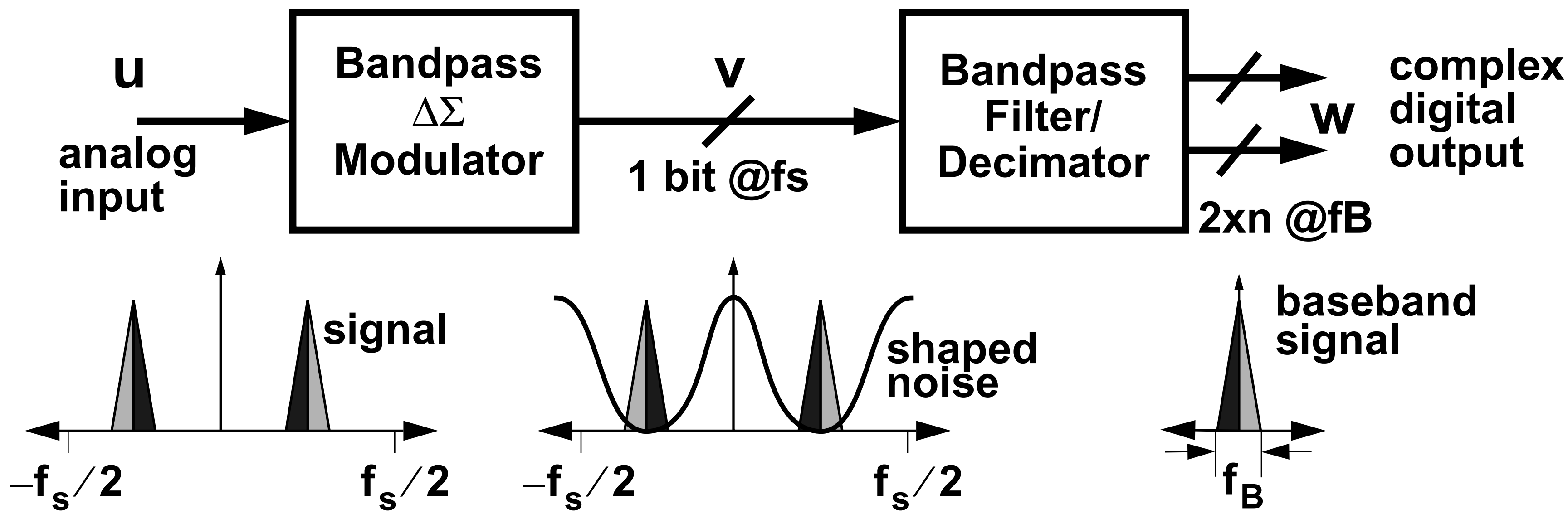
Click on Control Systems, then delsig



3. Bandpass ΔΣ

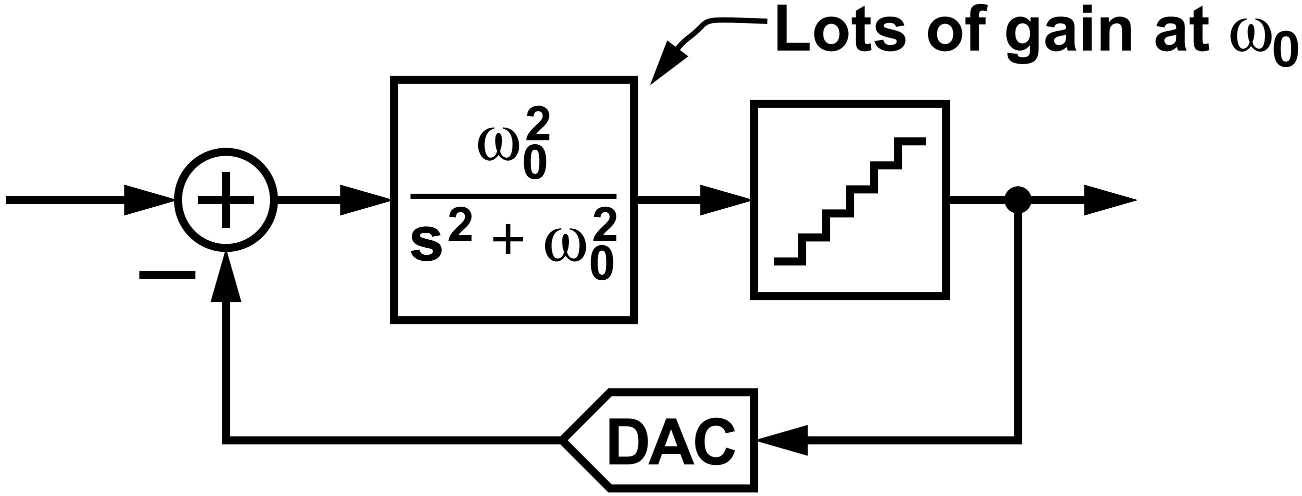
A Bandpass ΔΣ ADC

- **Like a lowpass ΔΣ ADC, a bandpass ΔΣ ADC converts its analog input into a bit-stream**
  - **The output bit-stream is essentially equal to the input in the band of interest.**
- **A digital filter removes out-of-band noise and mixes the signal to baseband**



BPΔΣ Perspective #1
It is just Filtering and Feedback

- Putting the poles of the loop filter at ω_0 forces *H* to have zeros at ω_0
- Example system diagram:



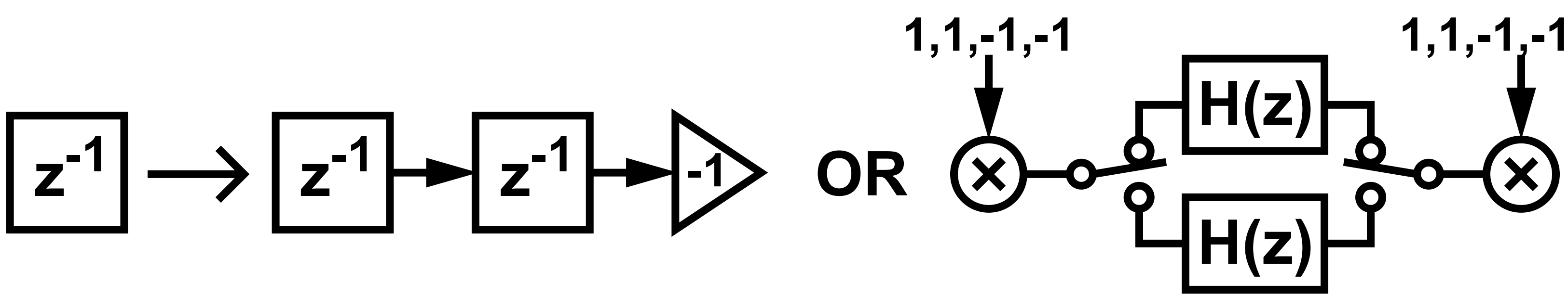
BPΔΣ Perspective #2

It is just the result of an "*N*-Path Transformation"

- $z \to -z^2$ (a "pseudo 2-path transformation") applied to $H(z) = 1 - z^{-1}$ yields $H'(z) = 1 + z^{-2}$
- This transformation can be applied to any system that processes DT signals, including SC filters, digital filters, ΔΣ modulators and even mismatch-shaping logic
  - By replacing the state storage elements (registers), or by interleaving two copies of the original system and negating alternate inputs and outputs

BPΔΣ Perspective #3
It is something New and Valuable

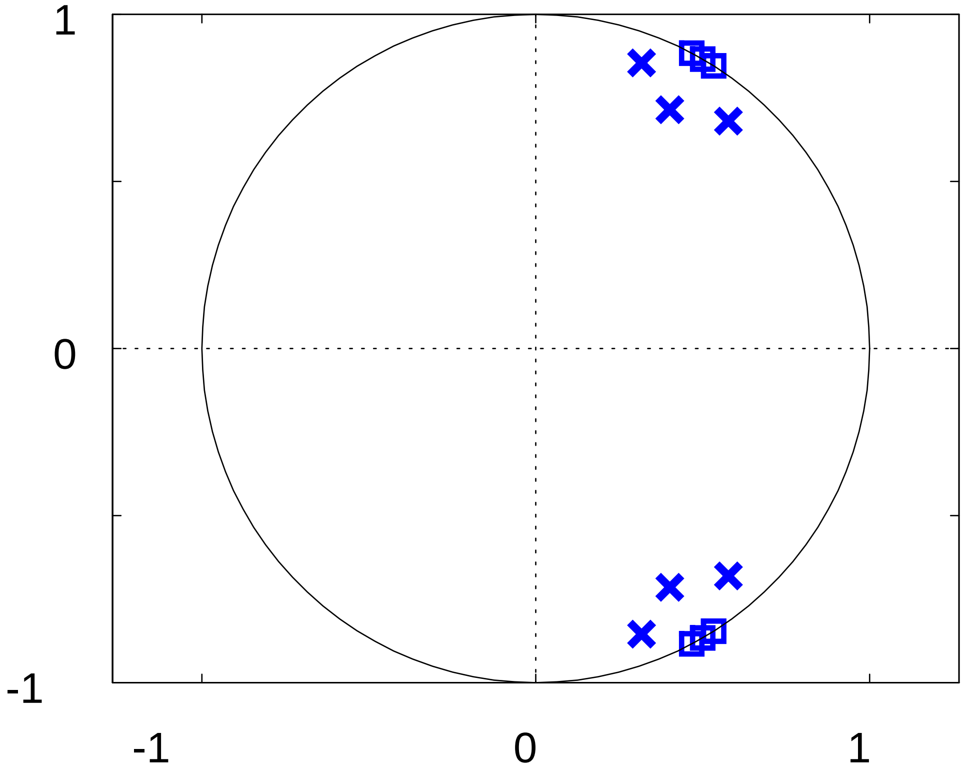
- **BPΔΣ offers a way to make a "tuned" ADC**
  - Possibly the only way.
  - Ideally-suited to narrowband systems, i.e. radios.
- **BPΔΣ keeps the signal away from 1/f noise as well as low-frequency distortion products**
  - Like regular narrowband bandpass systems, second-harmonic distortion is not problematic.



A 6^{th}-Order Bandpass NTF

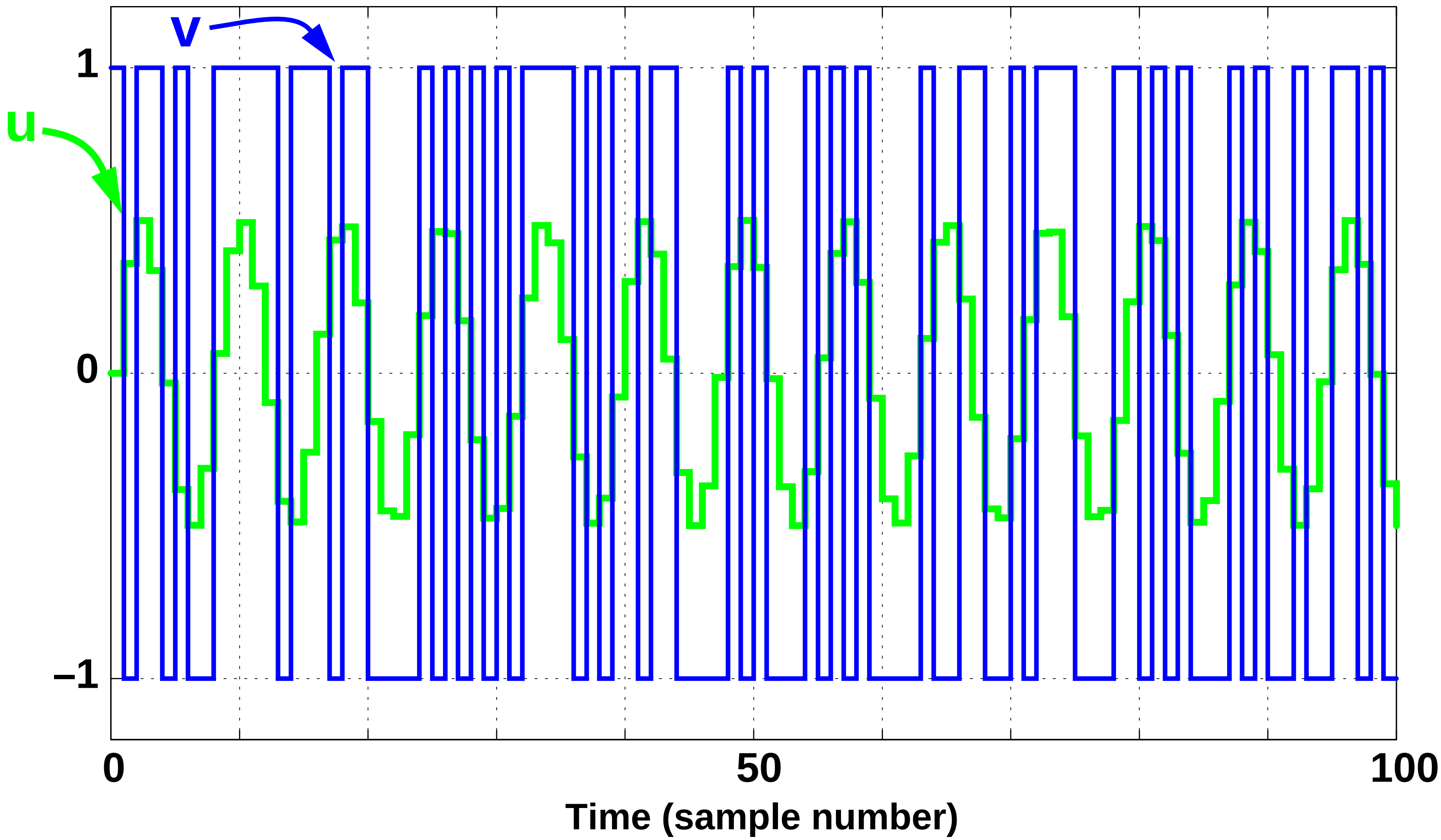
- **Pole/Zero diagram:**

```
OSR = 64;
f0 = 1/6;
H=synthesizeNTF(6,OSR,1,[],f0);...
```



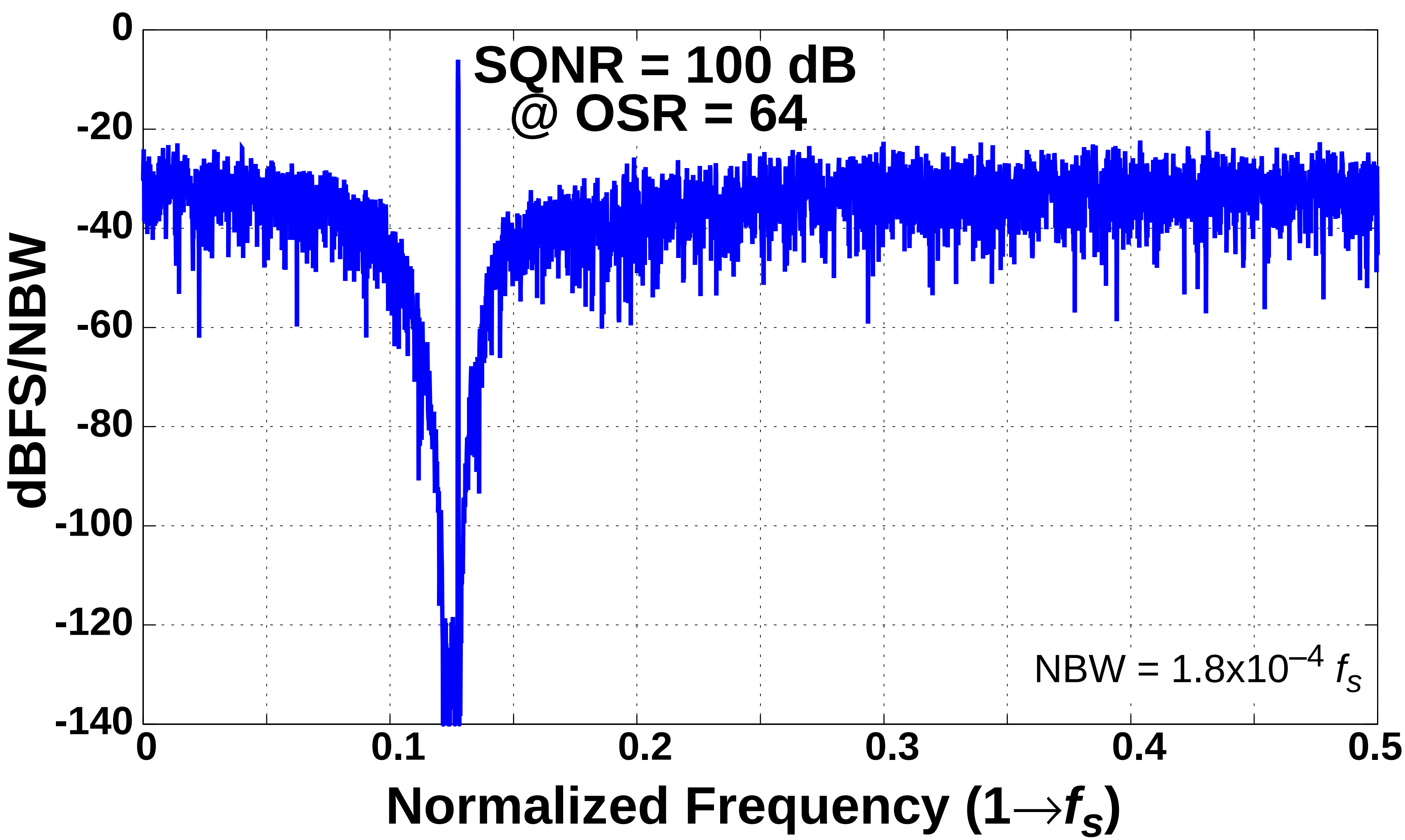
Example Waveform

8th-Order $f_s/8$ Bandpass Modulator

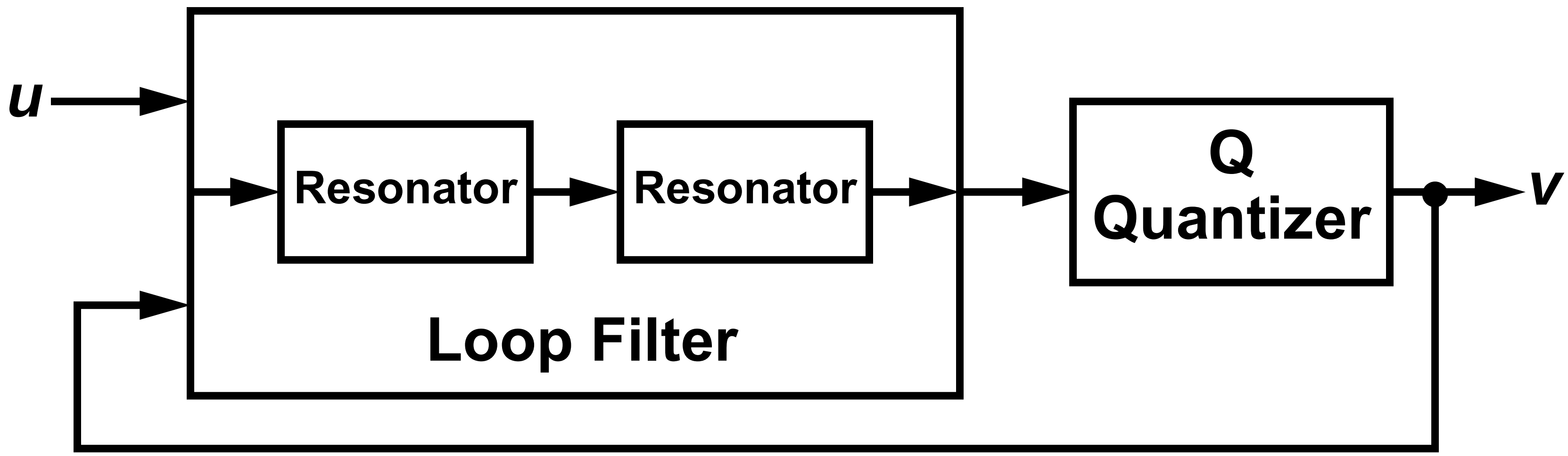


Example Spectrum

8th-Order f_s/8 Bandpass Modulator



Bandpass Modulator Structure



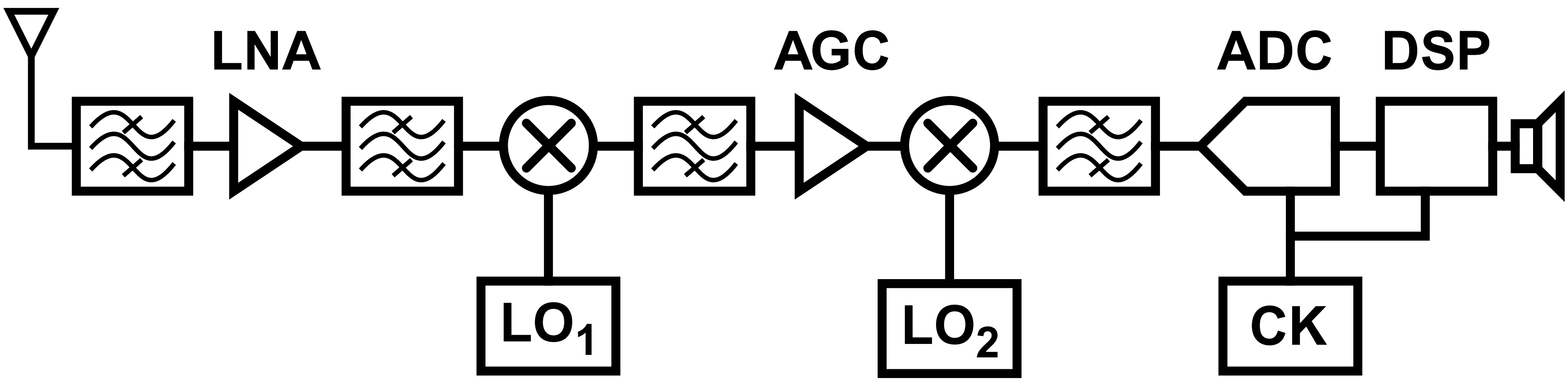
- **The loop filter consists of a cascade of resonators**

  The resonance frequencies determine the poles of the loop filter and hence the zeros of the NTF.

- **Multibit and multistage variants are also possible**

4. Design Example

A Dual-Conversion Superheterodyne Receiver



RF
50-2000 MHz

1st IF
10-300 MHz

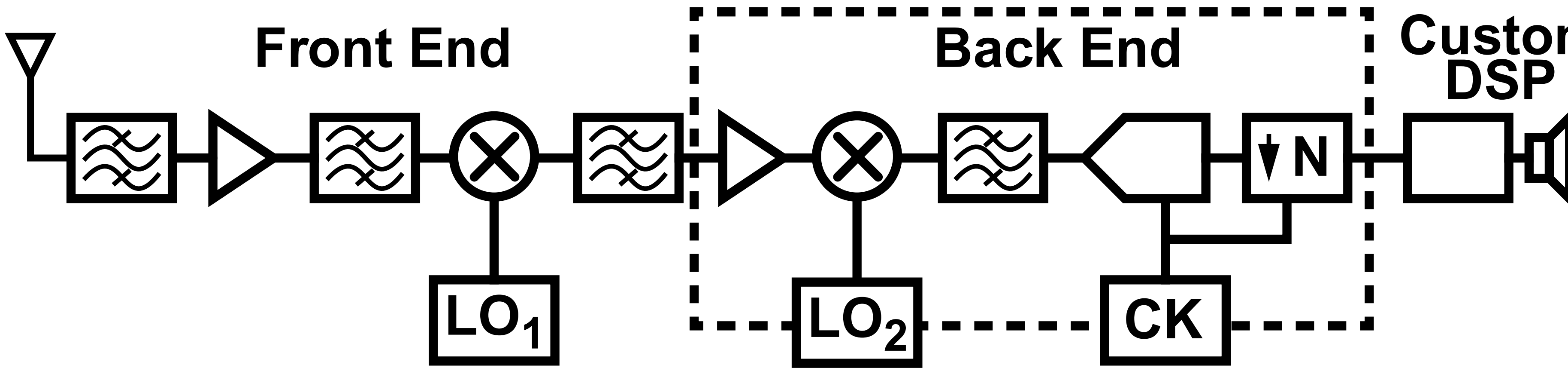
2nd IF
2-4 MHz

Sample Rate
10-750 ksps

- **A bandpass ADC fits naturally into this narrowband system**

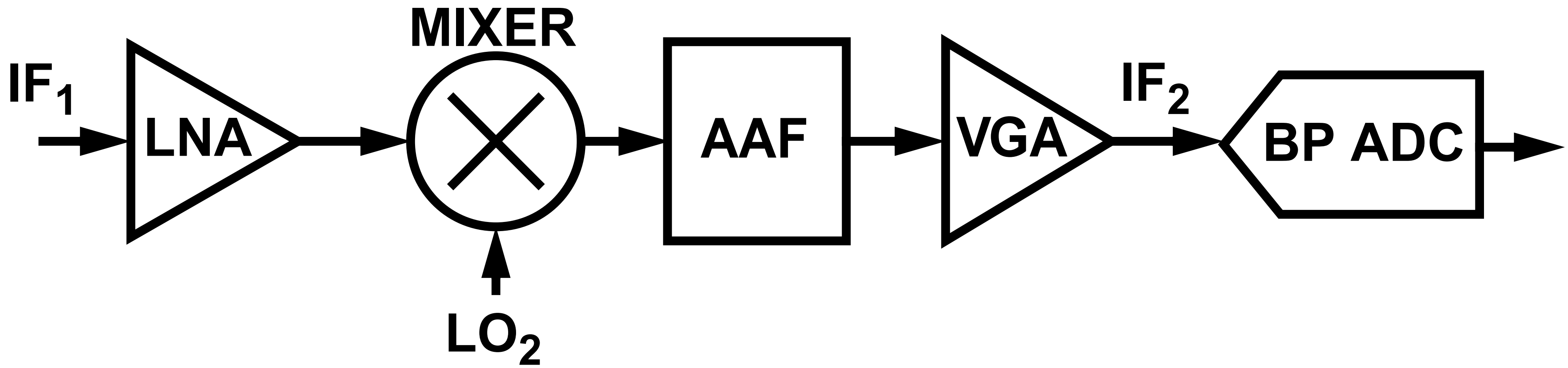
  Perfect I/Q, high dynamic range. Low power?

System Partitioning



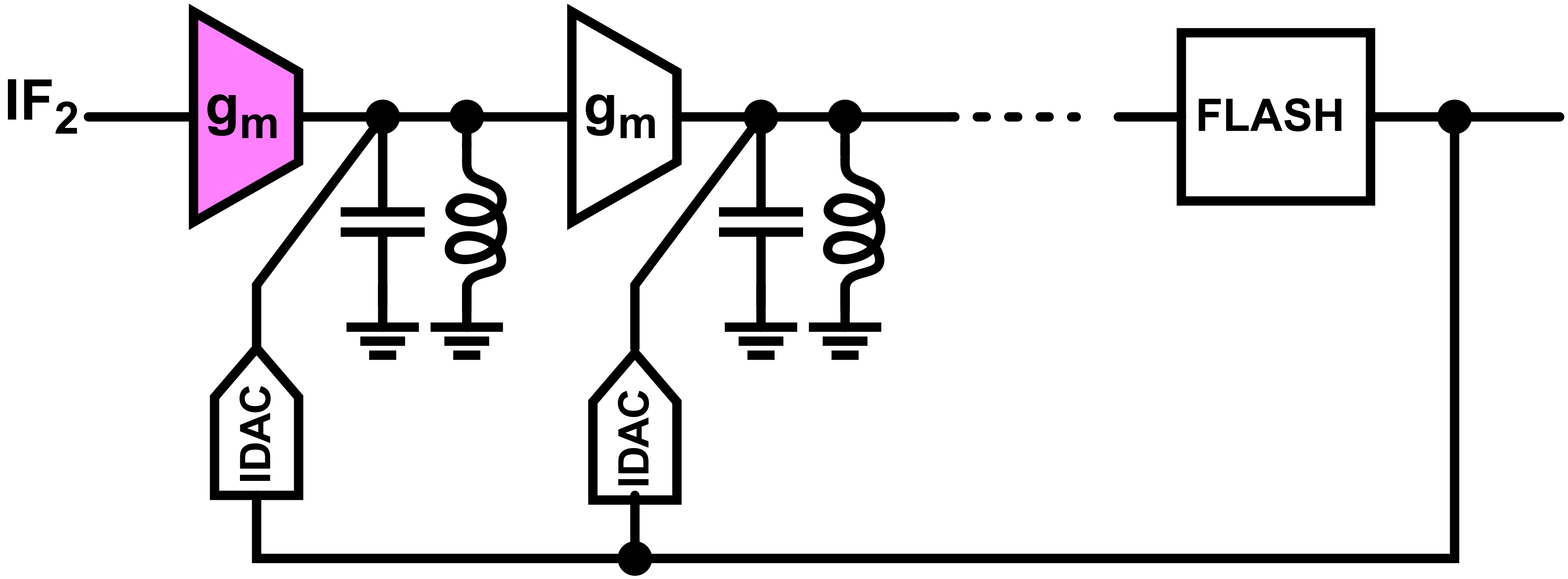
- **Goal: a general-purpose, high-performance, low-power back-end**

Traditional Implementation



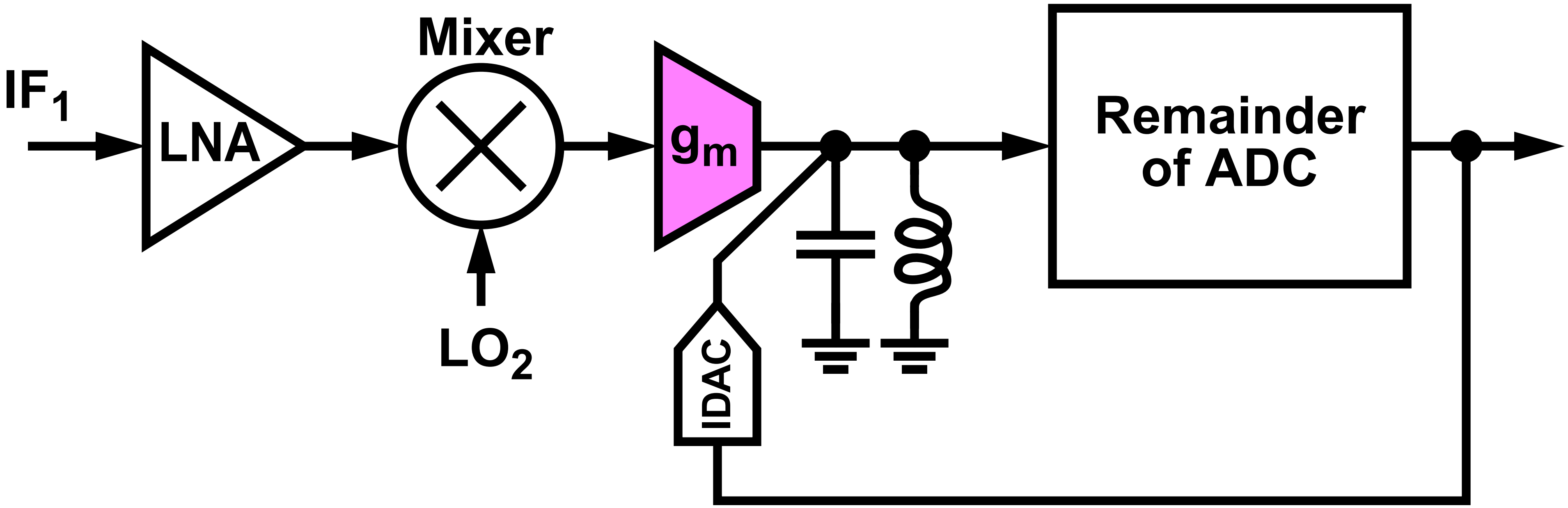
- ☹ Numerous high-dynamic range blocks
- ☹ Noise and power budgets are very tight
- ☹ Large VGA range needed

Eliminating the AAF with a Continuous-Time BP ΣΔ ADC



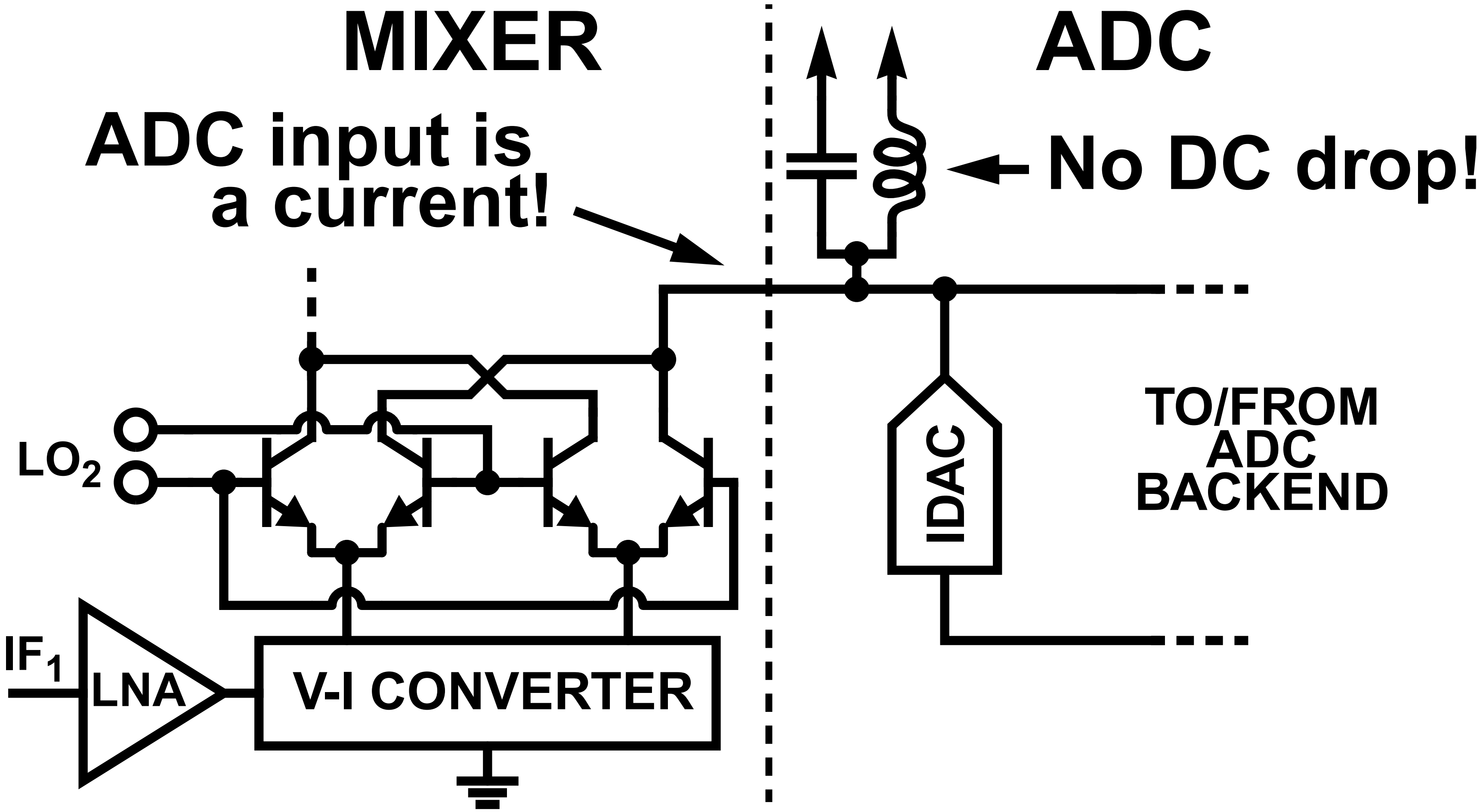
- ☺ Anti-alias filtering is inherent
- ☹ But still need a low-noise, linear V-I converter

Eliminating the Input g_m



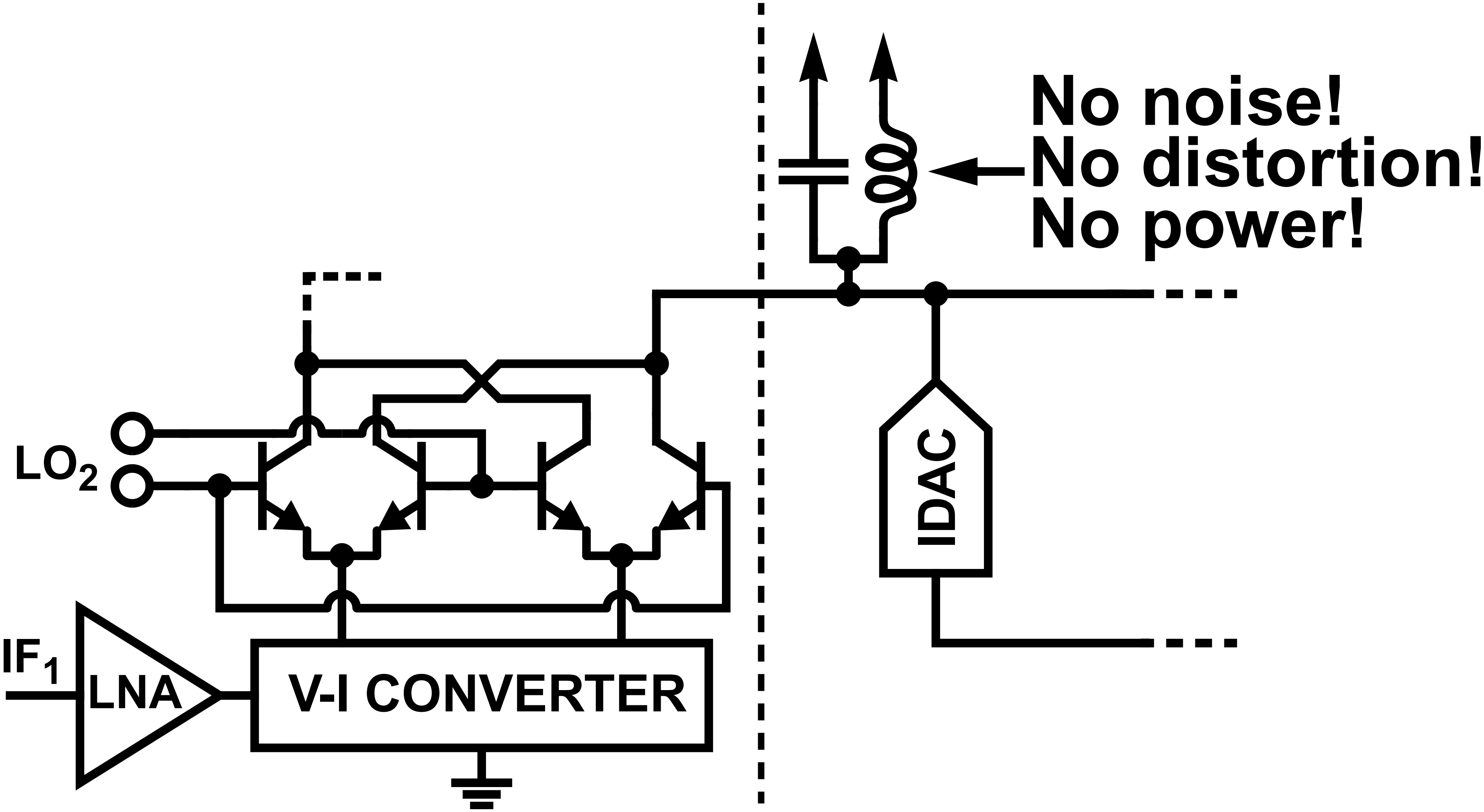
- **The output of the mixer is available in current form, so …**

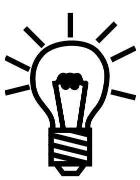
Merge ADC with Mixer!



- Eliminates redundant I-V & V-I conversion
- Gives mixer and IDAC more headroom

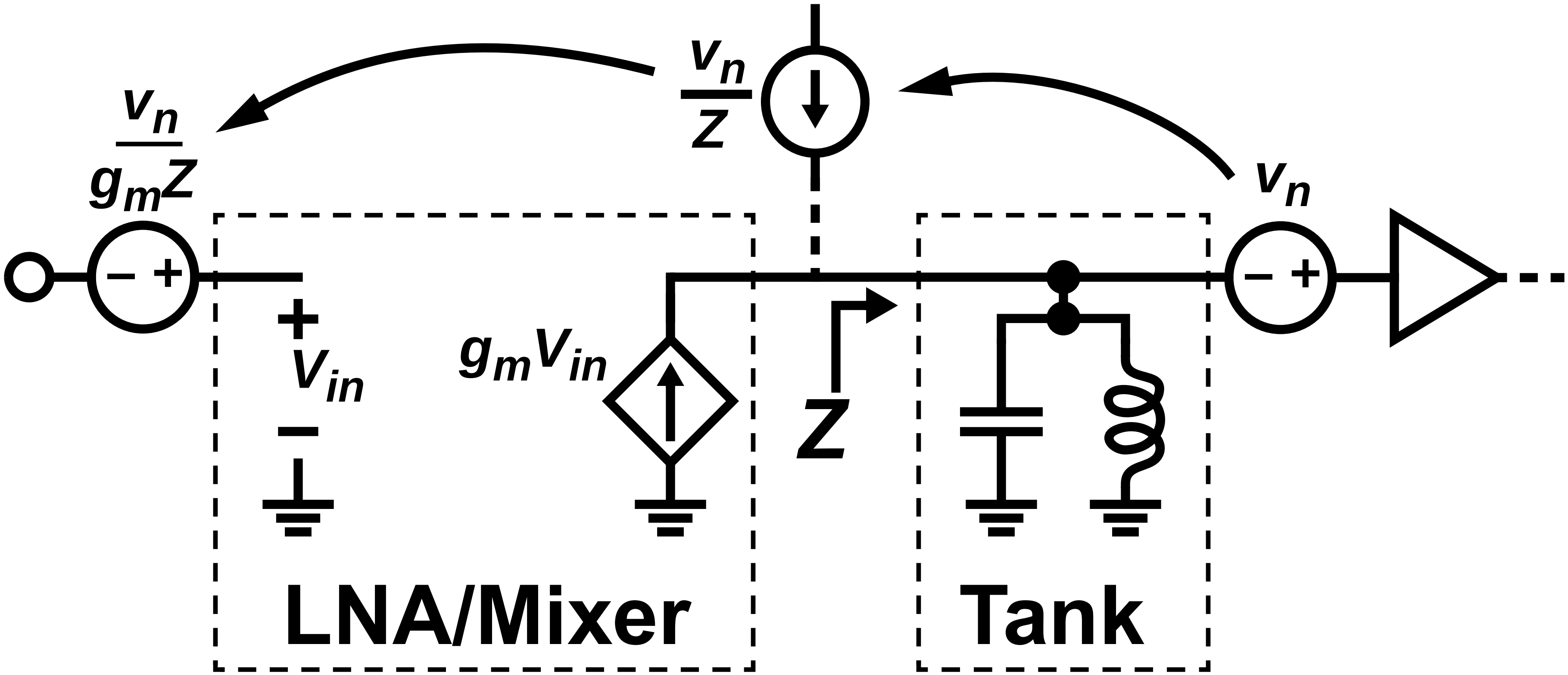
Merge ADC with Mixer!





LC tank effectively adds gain, without adding noise, adding distortion or consuming power

Noise Analysis



- **Noise in the ADC backend is attenuated by g_m times the tank impedance**
  - **In this work, $g_m \approx 10$ mA/V**

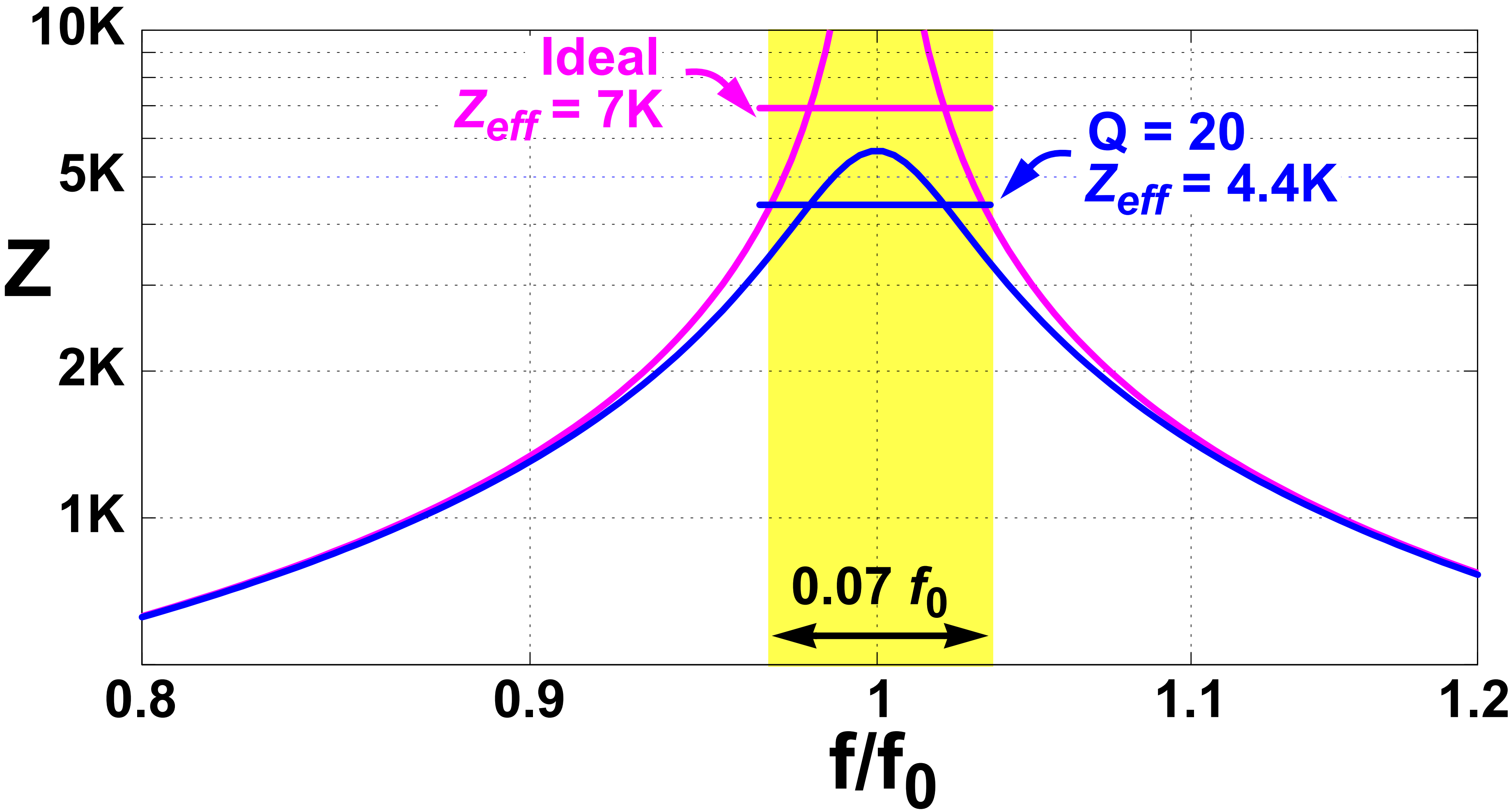
Z_{eff}

- **Near resonance, $|Z_L| = |Z_C|$**
  $|Z_{L,C}| \approx 300\Omega$ in this design
- **At resonance, $|Z| \approx Q \bullet |Z_{L,C}|$**
  About 6kΩ for $Q = 20 \Rightarrow g_m Z \approx 60$.
- **More generally, the effective tank impedance is found by integrating the input-referred noise over the band of interest:**

$$\int \left(\frac{v_n}{g_m Z(\omega)}\right)^2 d\omega = \left(\frac{v_n}{g_m}\right)^2 \int Y(\omega)^2 d\omega = \left(\frac{v_n}{g_m Z_{eff}}\right)^2$$

$$\Rightarrow Z_{eff} = (Y_{rms})^{-1}$$

Z vs. Frequency

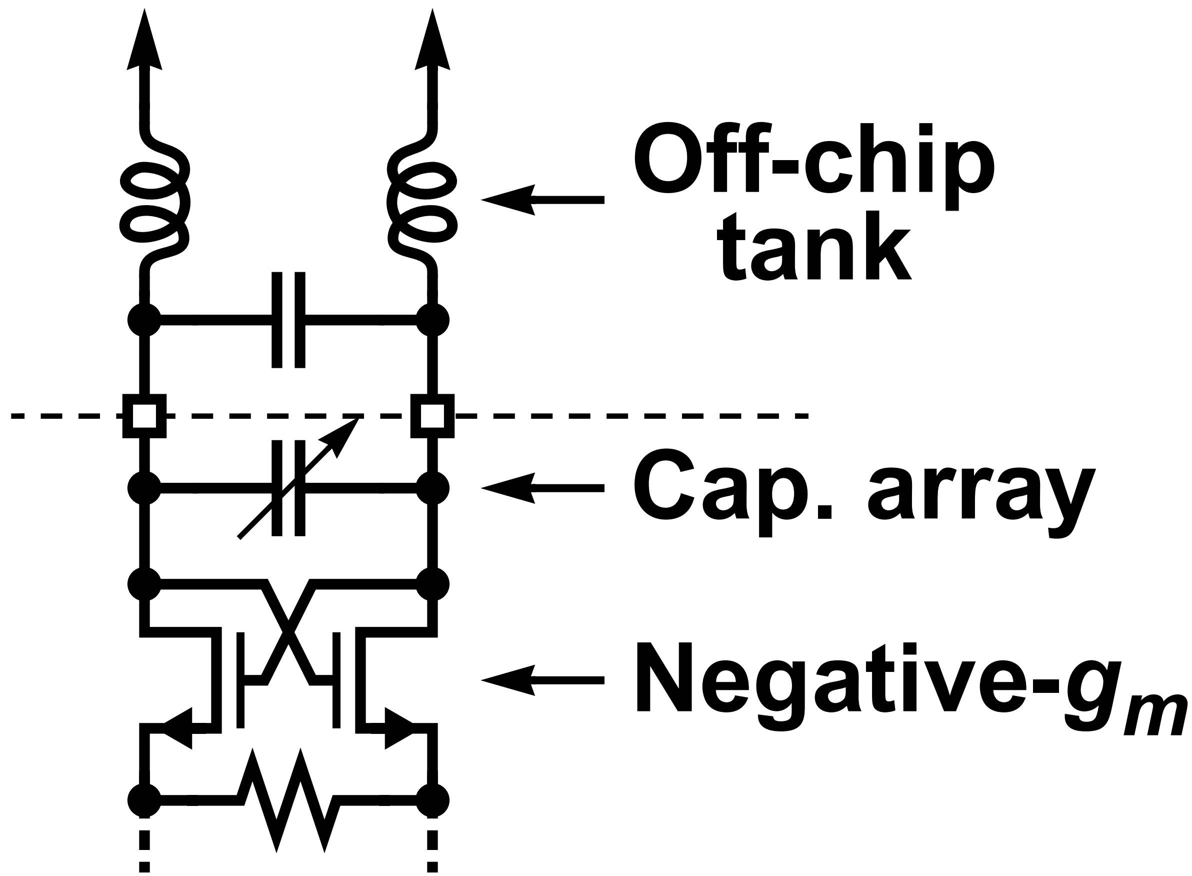


- Q = 20 reduces Z_{eff} by about 4 dB

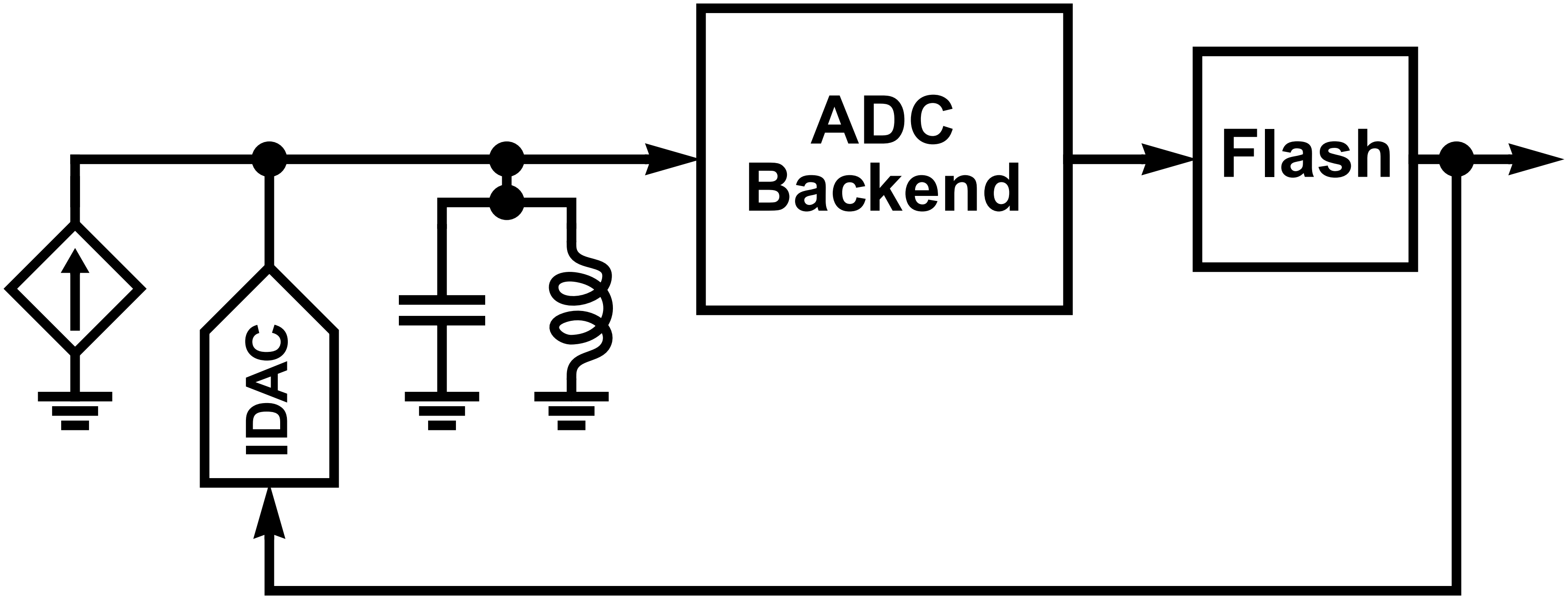
Tuning the LC Tank

- $\Delta f_0/f_0 = 2\% \Rightarrow$ 3 dB reduction in Z_{eff}
  Inductor accuracy is 10%, so tuning is required

Make an oscillator:

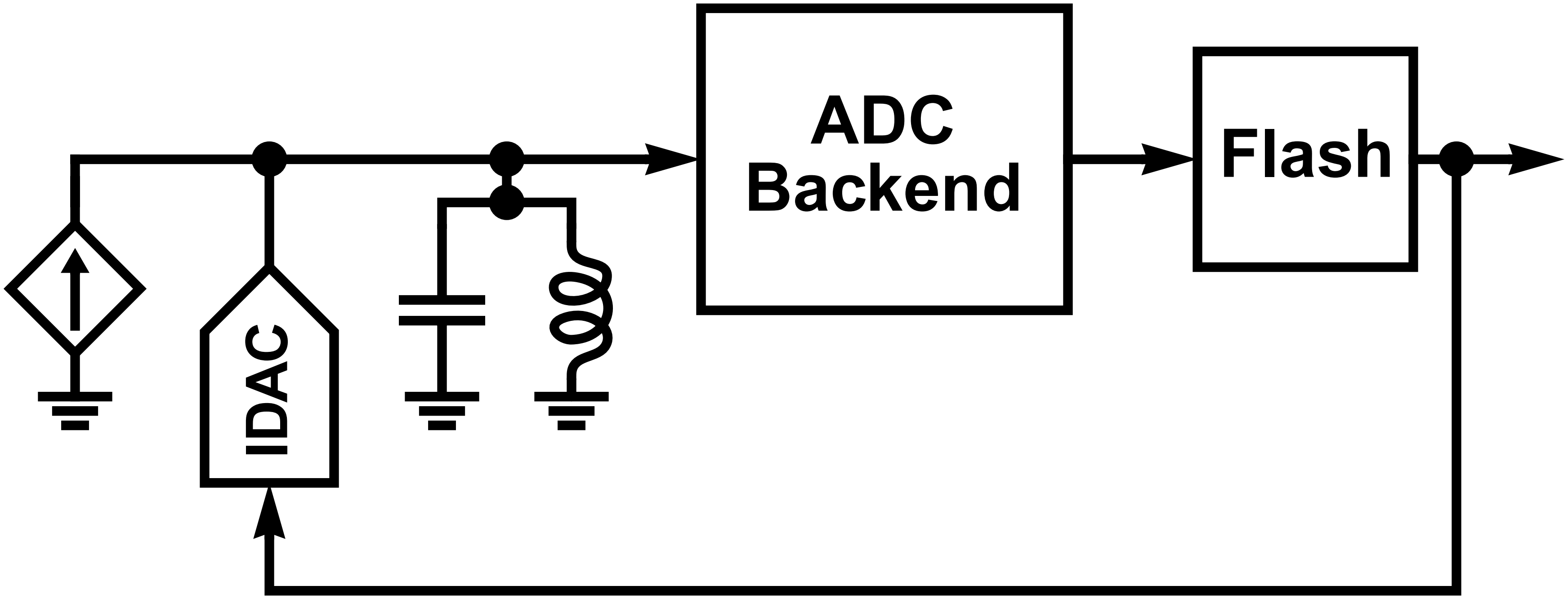


Remainder of ADC?



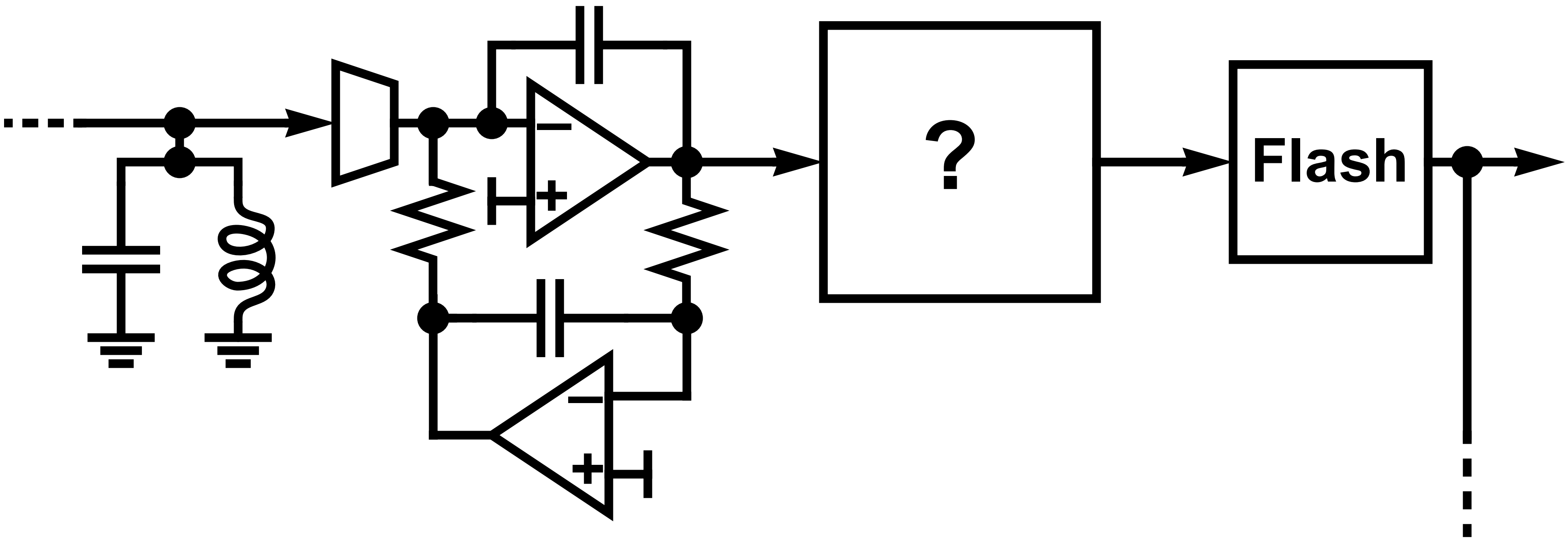
- **Add resonator stages until the quantization noise of the flash is low enough**

Second Resonator?



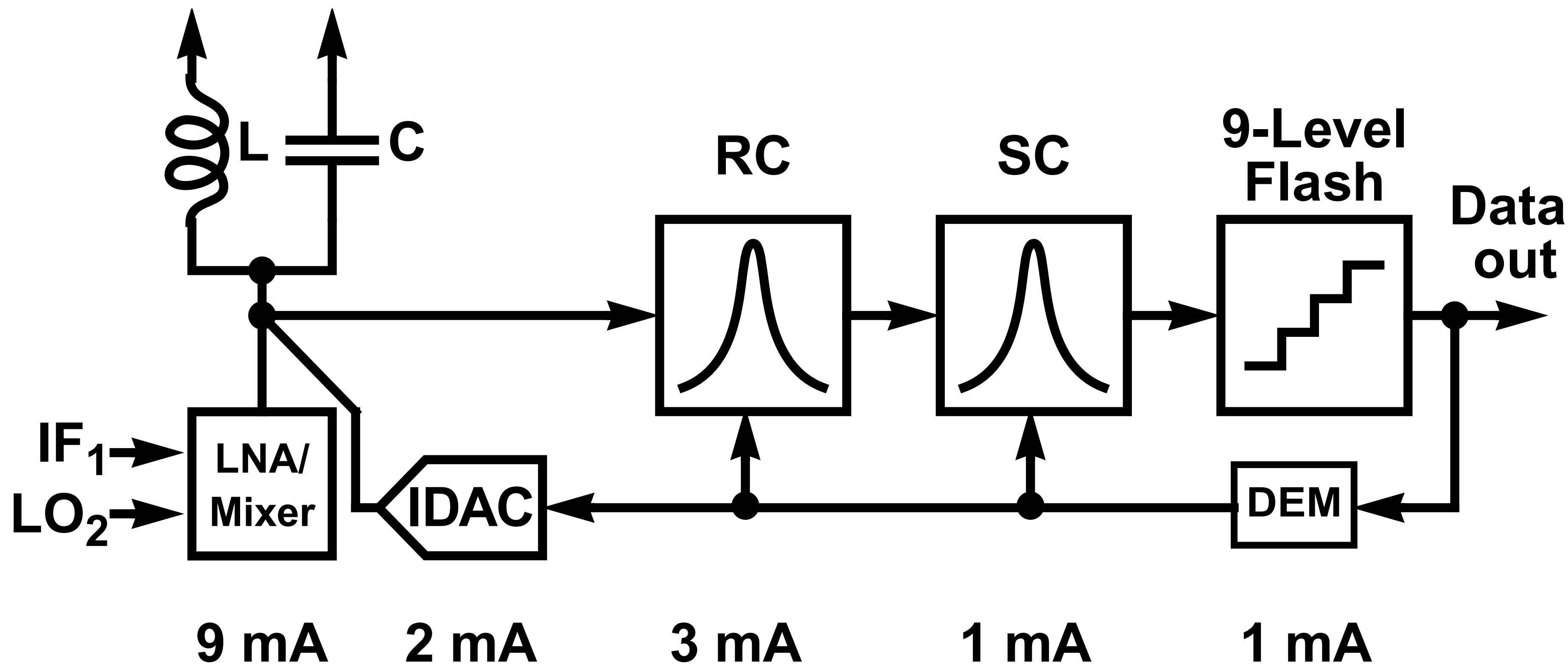
- LC: Needs more external components plus associated pins
- Active-RC: 2 mA for 50 nV/$\sqrt{Hz}$ input-referred noise
- Switched-Cap: est. >10 mA for same noise

Third Resonator?



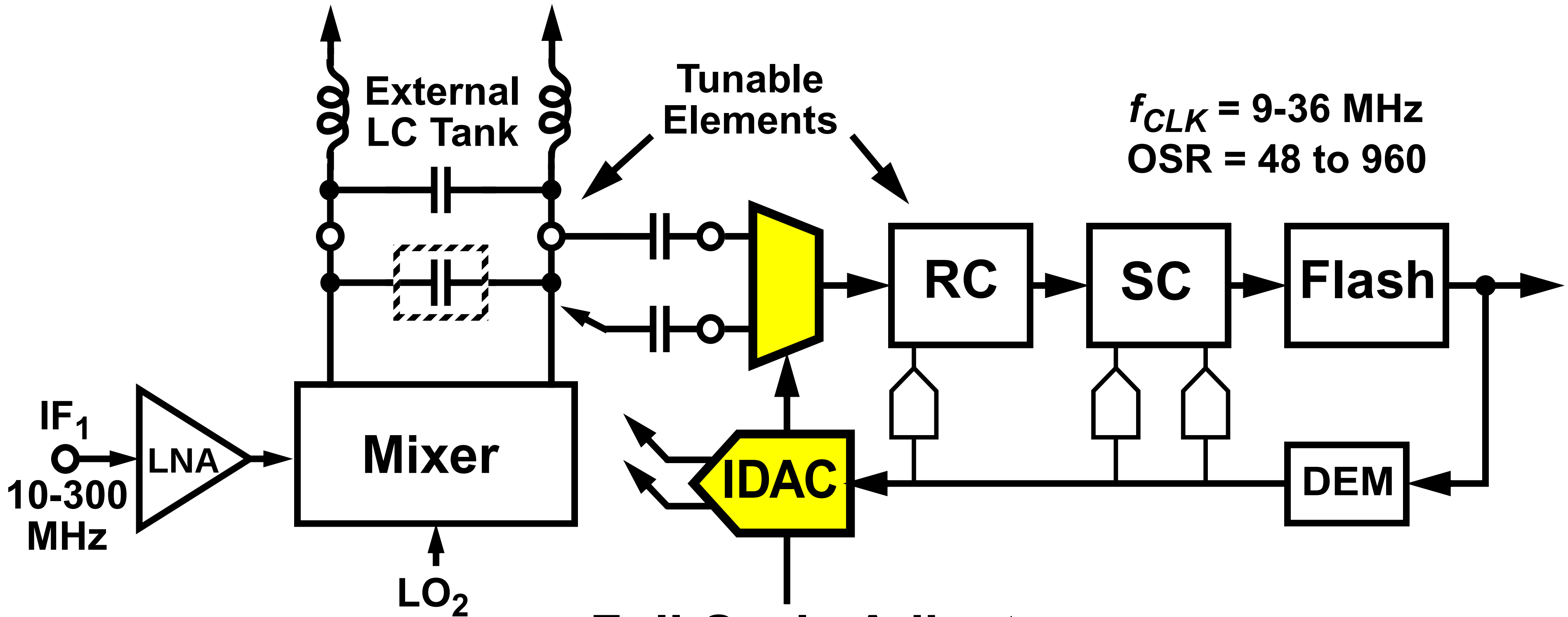
- **Active-RC: $Q \approx 10 \Rightarrow$ Need 4th resonator**
- **Switched-Cap: Q is high & drift is low;**
  <1 mA for 300 nV/$\sqrt{Hz}$ i.r.n.

Complete ADC



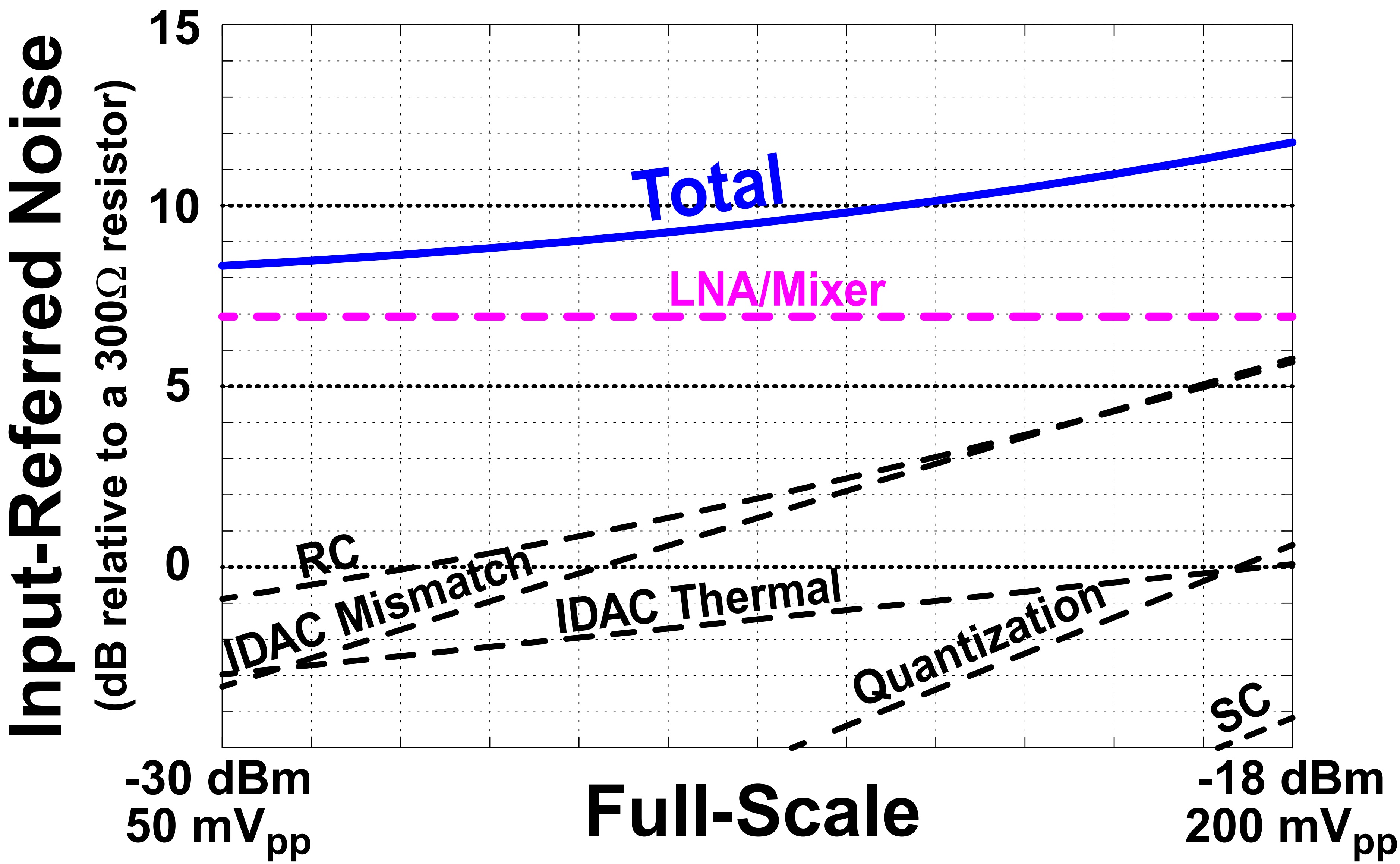
- **Eliminates high-power VGA & AAF**
  2/3 of the total power used by LNA, Mixer & IDAC
- **Uses cts-time and discrete-time elements, plus multi-bit quantization and mismatch-shaping**

ADC in More Detail

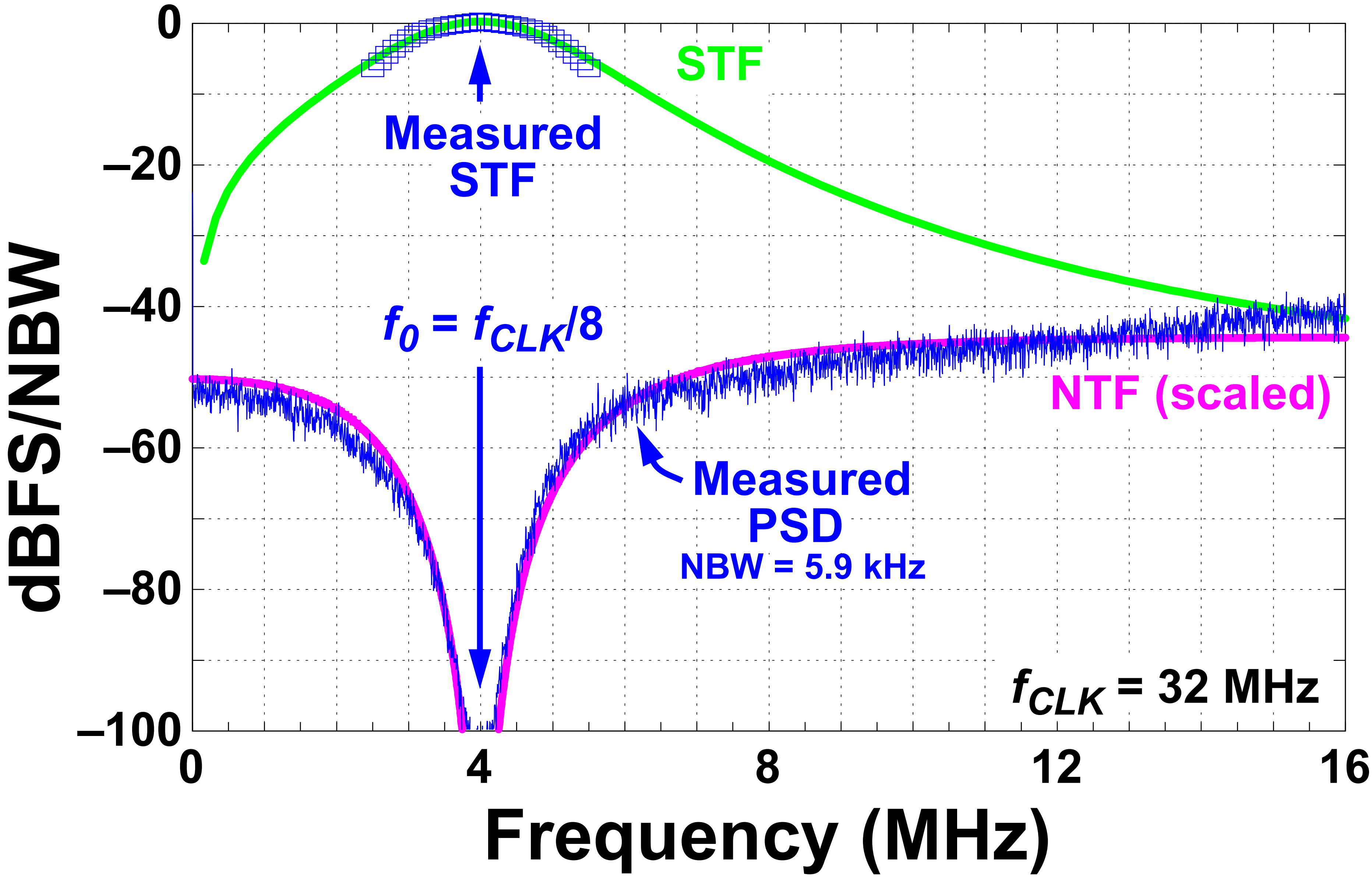


- **Can save power under small-signal conditions by reducing IDAC's full-scale**
  By a factor of 4, in this ADC

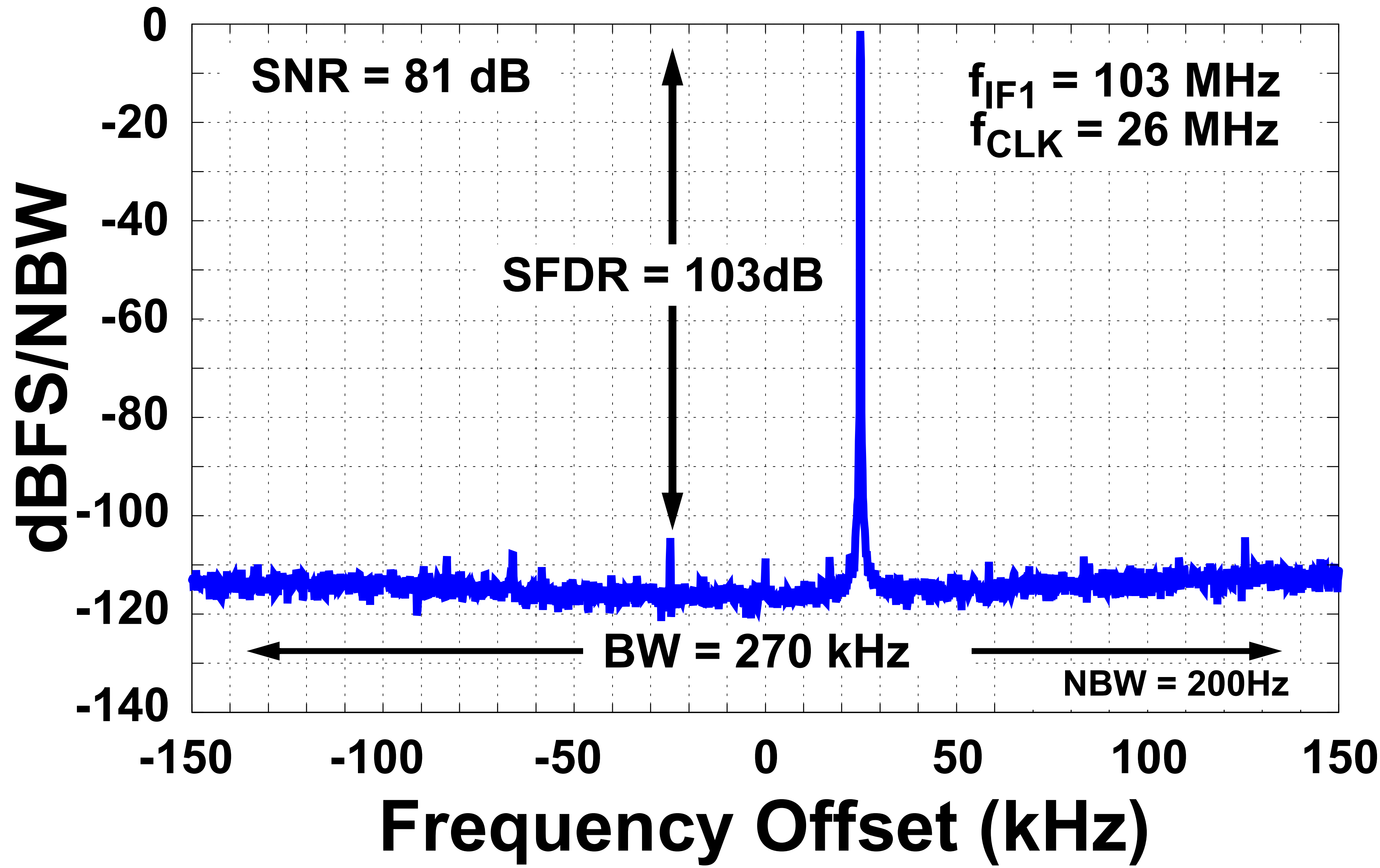
Noise vs. Full-Scale



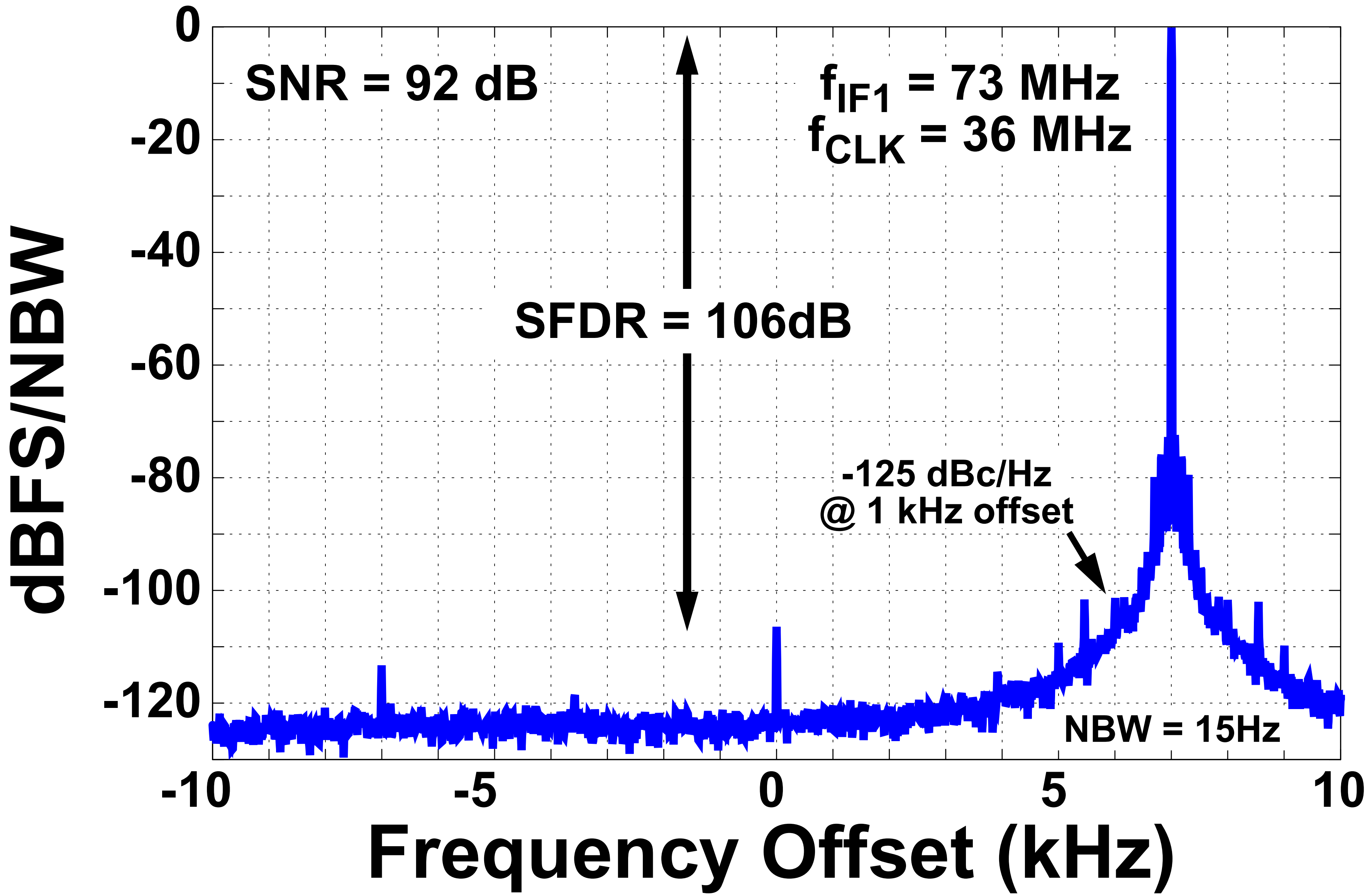
Measured STF & NTF



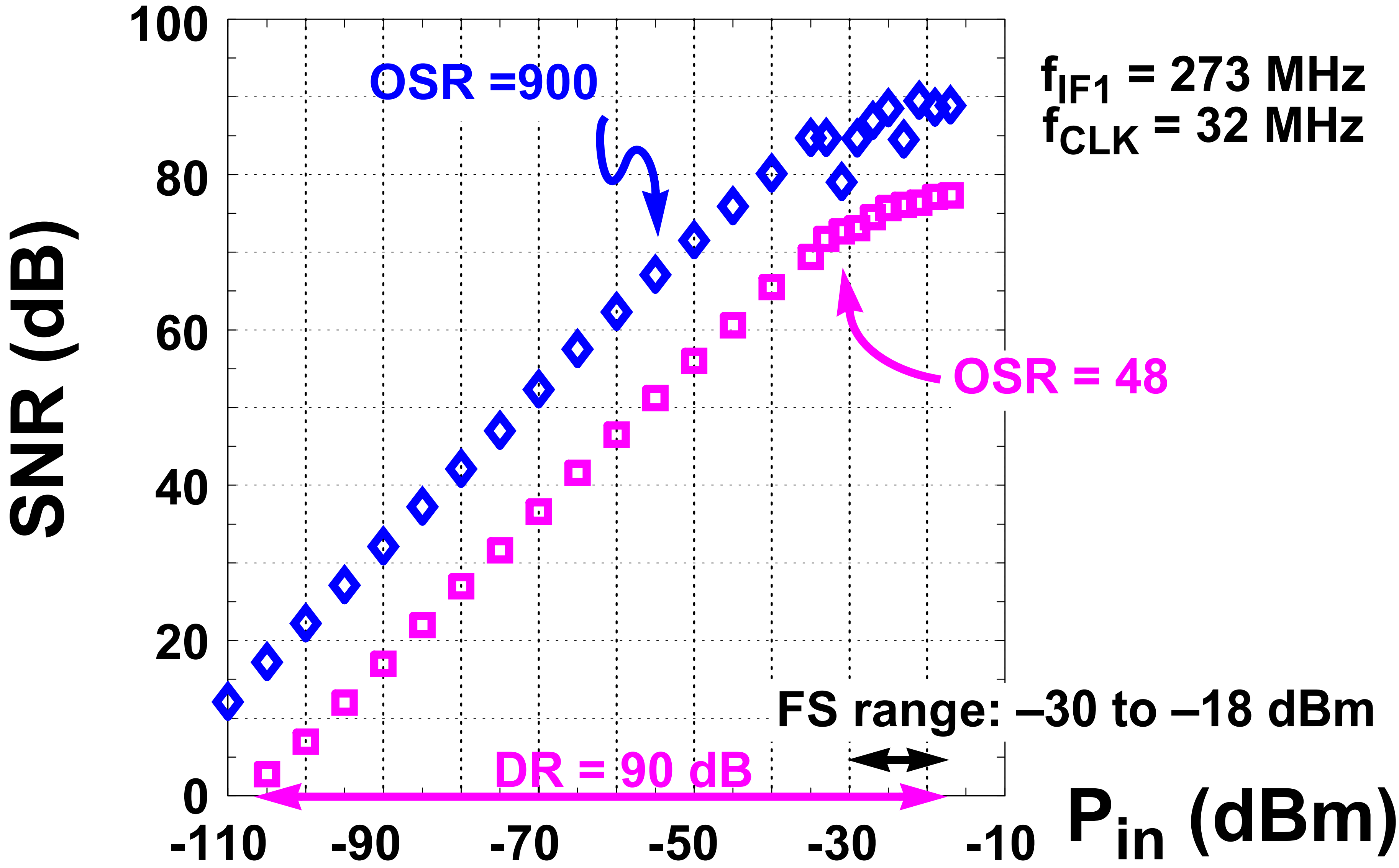
In-Band Spectrum (OSR=48)



In-Band Spectrum (OSR=900)



SNR vs. Input Power



Architectural Highlights

- **Merging a mixer with a continuous-time bandpass ADC containing an LC tank yields a flexible, high-performance, low-power receiver backend.**

- **Performing a component-count/performance/ power trade-off in each resonator section results in a multi-bit, hybrid continuous-time/discrete-time architecture.**

- **A variable full-scale saves power *and* reduces noise.**

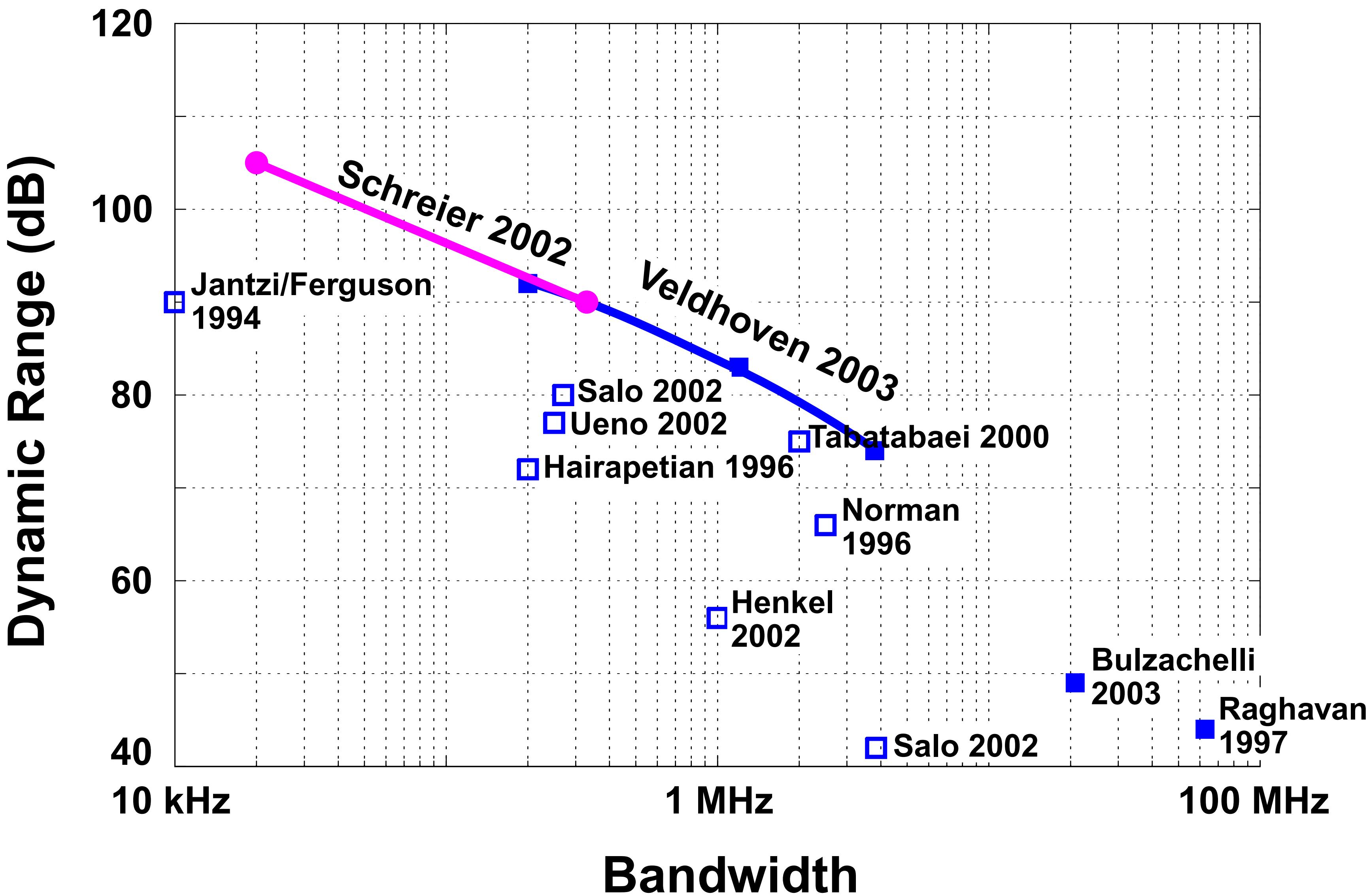
Performance Summary

Bandwidth	5 - 375	kHz
Input Frequency	10-300	MHz
Clock Frequency	9 - 36	MHz
Full-Scale Range	12	dB
Die Area	5	mm^2

@ f_{IF} = 73MHz, BW = 333kHz, f_{CLK} = 32MHz, VDD = 3V:

Dynamic Range	90	dB
Current Consumption	16.5	mA
Noise Figure @ min FS	9	dB
IIP3	0	dBm

Bandpass ΔΣ ADCs



Summary

- $\Delta\Sigma$ is fun
  - All kinds of exotic behavior: limit-cycles, dead-bands sub-harmonic locking and even chaotic dynamics!
- $\Delta\Sigma$ is a rich field
  - ADCs and DACs; Single-bit and Multi-bit; Single-stage and Multi-stage; Lowpass and Bandpass; Discrete-time and Continuous-time…
- A bandpass $\Delta\Sigma$ ADC converts an IF signal into digital form and can do so with high dynamic range and low power consumption
  - With wideband or tunable modulators, conversion of RF to digital may soon be feasible.
  - ADC = “Antenna to Digital Converter”