Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

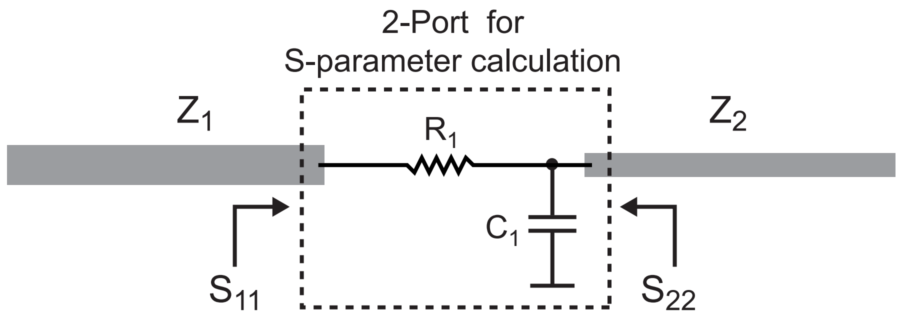
6.976 High Speed Communication Circuits and Systems

Mid-Term Exam

Name______________________________

Problem 1	______________
Problem 2	______________
Problem 3	______________
Problem 4	______________
Total	______________

1. (20 points) Consider the circuit network connected to lossless transmission lines of characteristic impedance Z_1 and Z_2 as shown in the figure below. Assume in all cases that Z_1 and Z_2 are purely real.



a. Derive an expression for S_{11} in terms of Z_1, Z_2, R_1, and C_1.

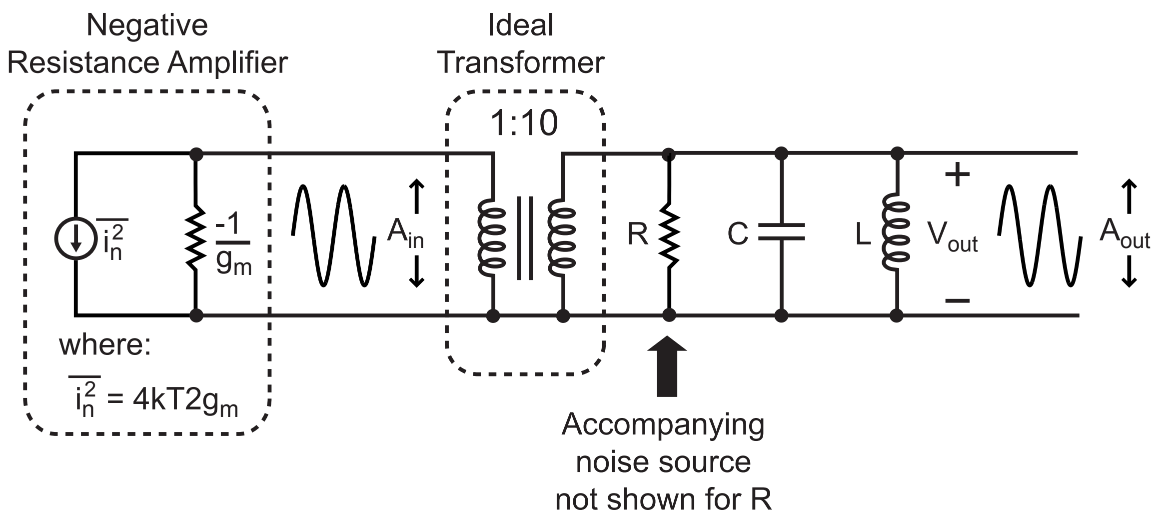
b. Derive an expression for S_{22} in terms of Z_1, Z_2, R_1, and C_1.

c. Derive an expression for S_{21} in terms of Z_1, Z_2, R_1, and C_1.

d. Consider the case where a pulse is launched down the left transmission line (with impedance Z_1). Will the initial portion of the voltage reflection back down the left transmission line be positive, negative, or zero given Z_1 = 50 Ohms, R_1 = 75 Ohms, C_1 = 1 pF, and Z_2 = 100 Ohms? Explain your answer.

e. Consider the case where a pulse is launched down the right transmission line (with impedance Z_2). Will the initial portion of the voltage reflection back down the right transmission line be positive, negative, or zero given Z_1 = 50 Ohms, R_1 = 75 Ohms, C_1 = 1pF, and Z_2 = 100 Ohms? Explain your answer.

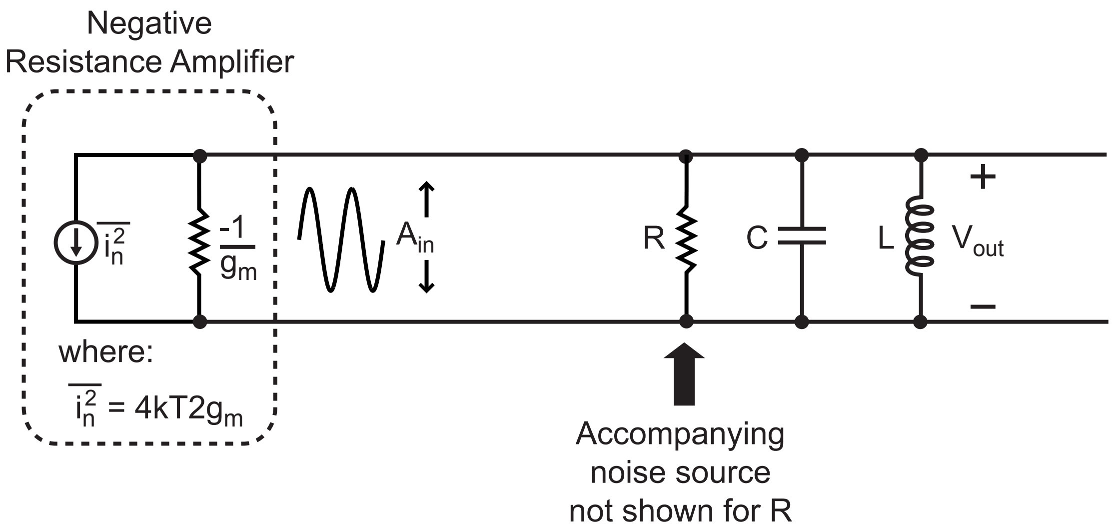
2. (25 points) Now consider the linearized VCO model shown in the figure below.



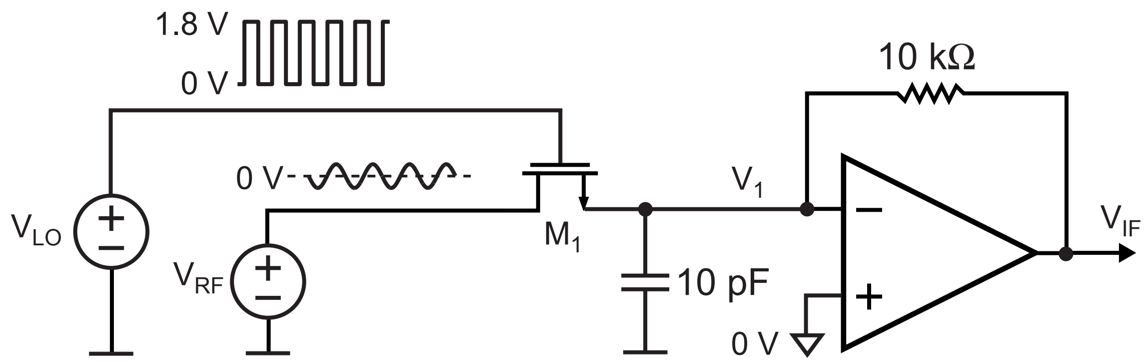
a. Calculate the value of g_m for the negative resistance amplifier for which steady-state oscillation is achieved.

b. Given the linearized VCO model illustrated on the previous page, derive an expression for the phase noise of the oscillator, L(Δf). Your expression should be a function of A_{in}, R, Q of the tank, and kT.

c. State the difference (in dB) between the minimum phase noise that can be achieved with the oscillator shown in the initial figure of this problem versus the oscillator shown below. Assume that the voltage swing at the active element output, A_{in}, is constrained in value to 2 V for both VCO structures, whereas the voltage across the tank itself is not constrained in either case.



3) (25 points) Consider the CMOS mixer shown below. Assume for all parts in this problem that the frequency of the RF input, V_{RF}, is 900 MHz, while the frequency of the LO output, V_{LO}, is 1 GHz. Also assume for all parts that the opamp has zero offset voltage, infinite DC gain, and infinite unity gain bandwidth.



a. Calculate the conversion gain of the mixer given that the channel resistance of M_1 (from source to drain) is infinite when $V_{LO} = 0$ V, and equals 1 kΩ when $V_{LO} =$ 1.8 V.

b. Calculate IIP3 of the mixer (in units of peak voltage squared, V_p^2) given that the channel resistance of M_1 (from source to drain) is infinite when $V_{LO} = 0$ V, but equals the following expression when $V_{LO} = 1.8$ V:

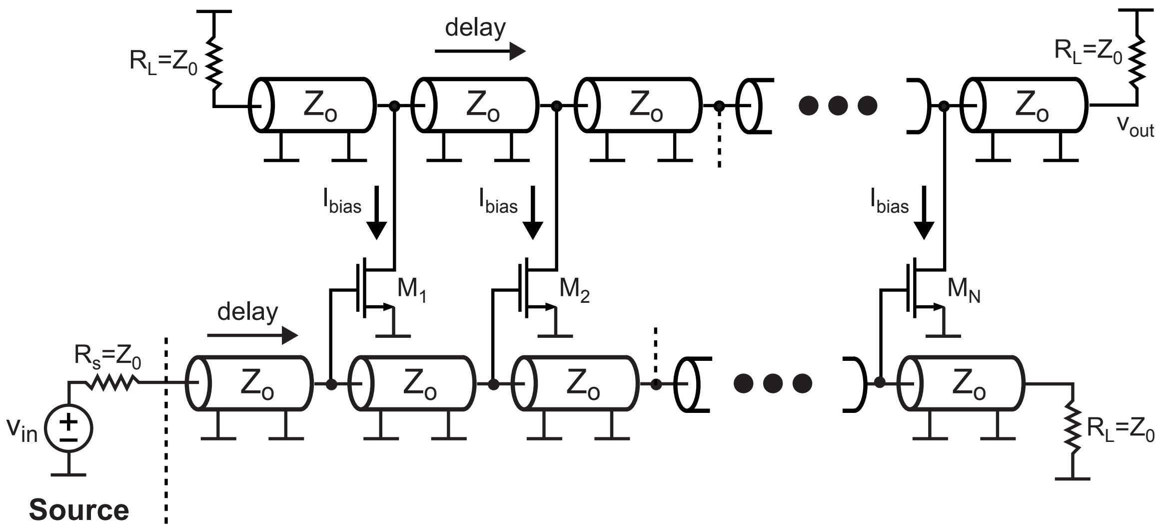
$$\text{Channel resistance} = dV_{ds}/dI_d = 1\ k\Omega/(V_{gs} - 0.8V - V_{ds}^2/2)$$

4) (30 points) Consider the distributed amplifier shown below consisting of N transistors whose input and outputs are connected through lossless transmission lines with characteristic impedance Z_0. For all parts to follow, ignore all loading effects of the transistors (i.e., ignore C_{gs}, C_{gd}, C_{db}, and r_o), and assume that all transmission line sections have equal delay. Also, ignore induced gate noise, and assume that the drain noise of each transistor is related to its transconductance as

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT2g_m$$

In addition, assume that a fixed current density is chosen for the transistors such that the transconductance for each transistor is related to its bias current as

$$g_m = \alpha \cdot I_{bias}$$



a. Compute the overall gain of the amplifier (v_{out}/v_{in}) as a function of the number of stages in the amplifier, N. Your answer should be expressed in terms of I_{bias}, α, Z_o, and N.

b. Compute the noise factor of the overall amplifier as function of N. Your answer should be expressed in terms of I_{bias}, α, kT, Z_o, and N.

Suppose that loading by the transistors can only be neglected if their individual area, A_t, is smaller than A_o. Assume that a specific current density is desired for each transistor such that its area is related to its bias current as

$$A_t = \beta \cdot I_{bias}$$

Given this constraint, derive expressions for the following parts (c) and (d)

c. Determine the minimum number of stages, N, that are required to achieve an overall amplifier gain (v_{out}/v_{in}) of G. For simplicity, assume that N does not need to be expressed as an integer value.

d. Suppose you desire to achieve the best noise factor given a fixed overall gain, G. Do you do better, worse, or the same for noise factor if you set N higher than the minimum value calculated in the previous part? Explain your answer.