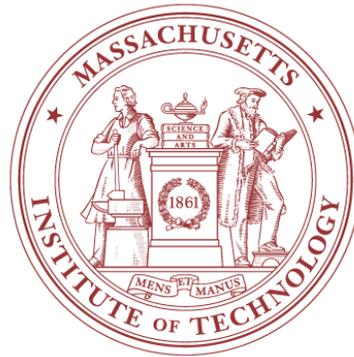


Modern Communication System Design: Course Overview

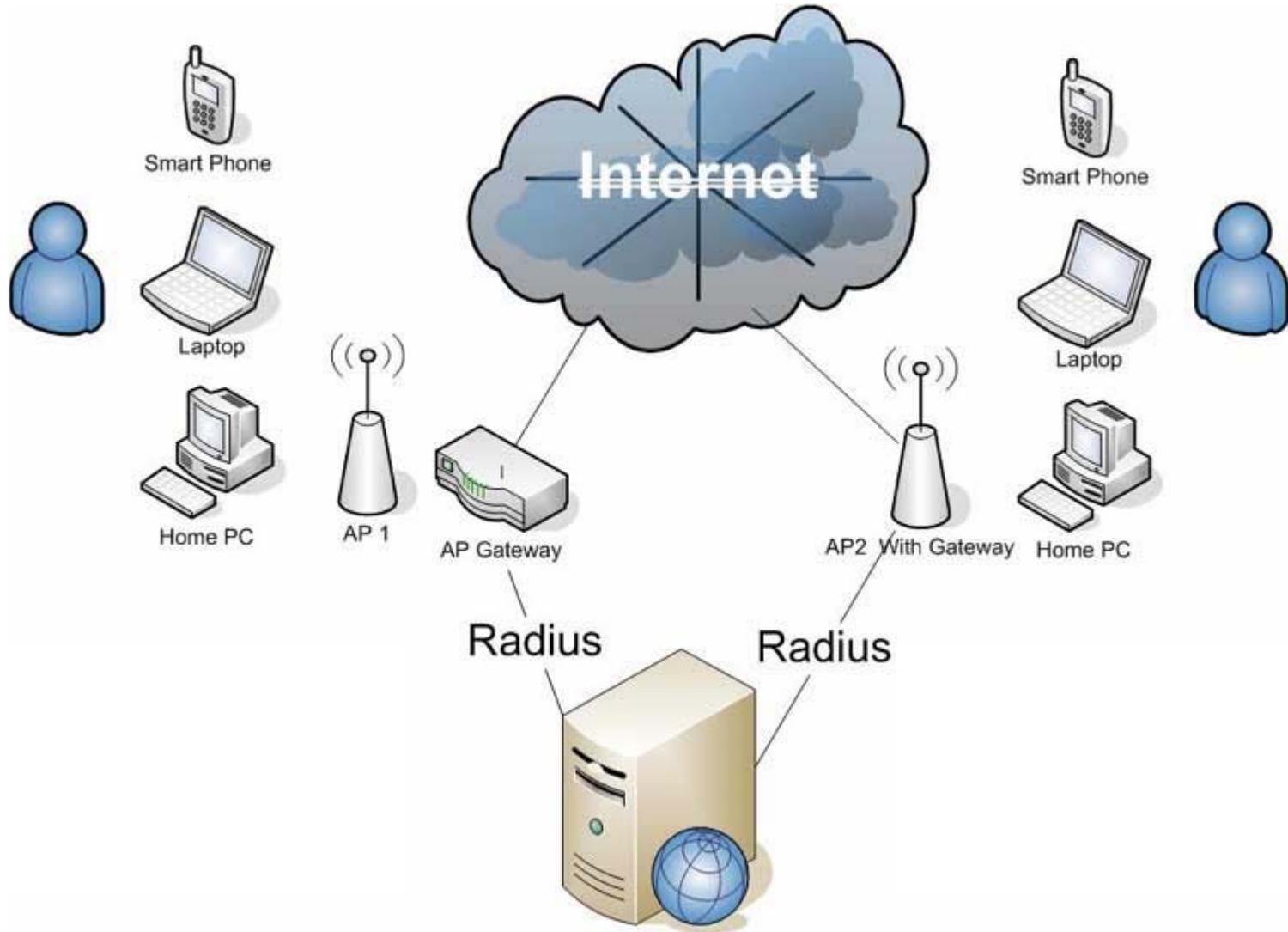
Lecture 1

Vladimir Stojanović



6.973 Communication System Design – Spring 2006
Massachusetts Institute of Technology

Communication systems are ubiquitous



Courtesy of Aradial Technologies. Used with permission.

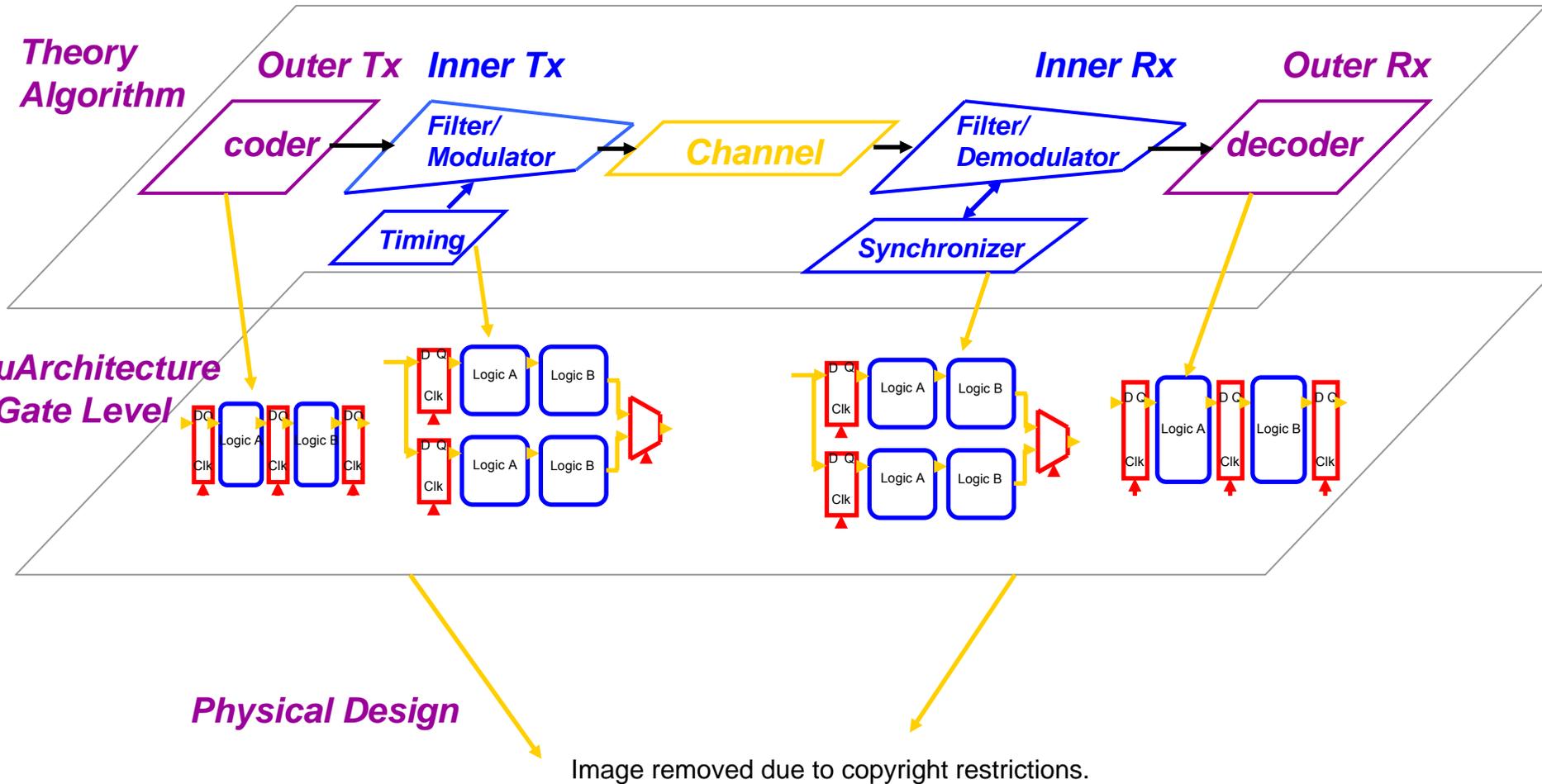
<http://www.aradial.com/images/hotspots.jpg>

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Very complicated – so divide & conquer



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Courses usually follow the hierarchy

- ❑ Not a bad thing
 - Get a lot of depth

- ❑ But, loose the “big picture”
 - Rarely get a chance to look at the whole system

- ❑ With today’s tight energy and performance specs
 - Need to optimize the whole system
 - Need to know and work **ACROSS** the hierarchy

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In 6.973 we'll try to cut ACROSS

- Project driver – Wi-Fi chip

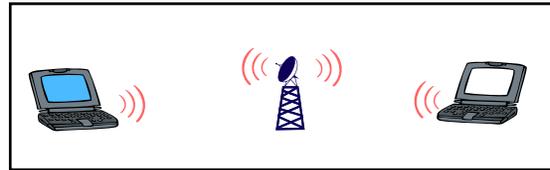
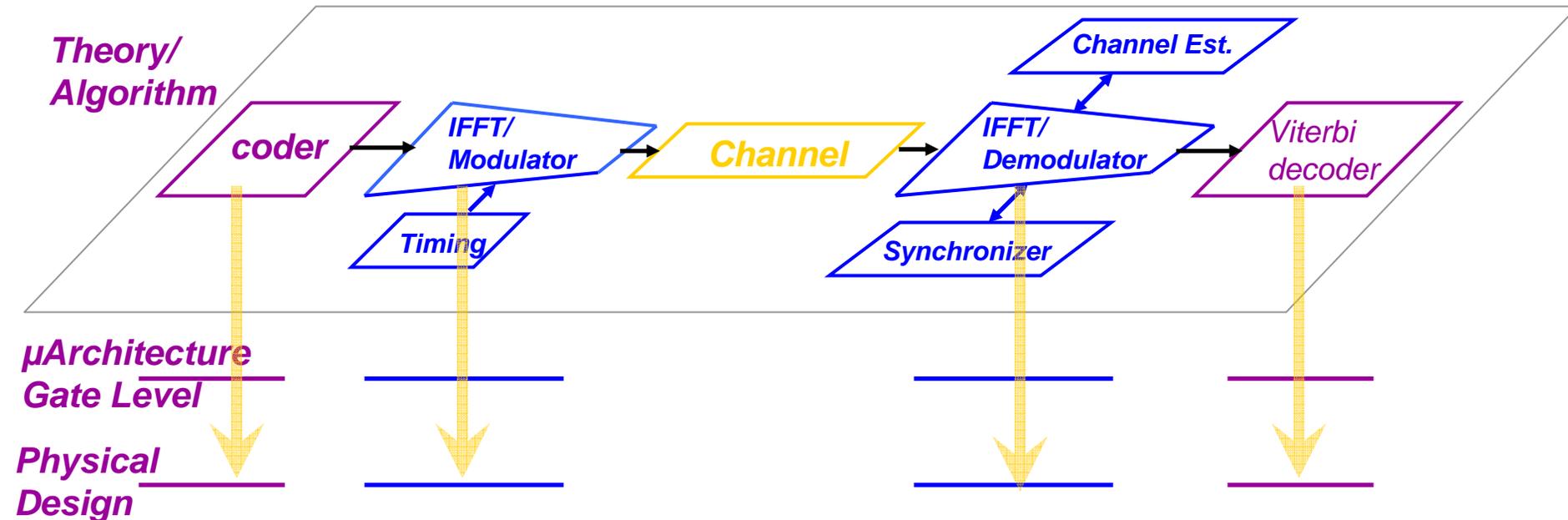
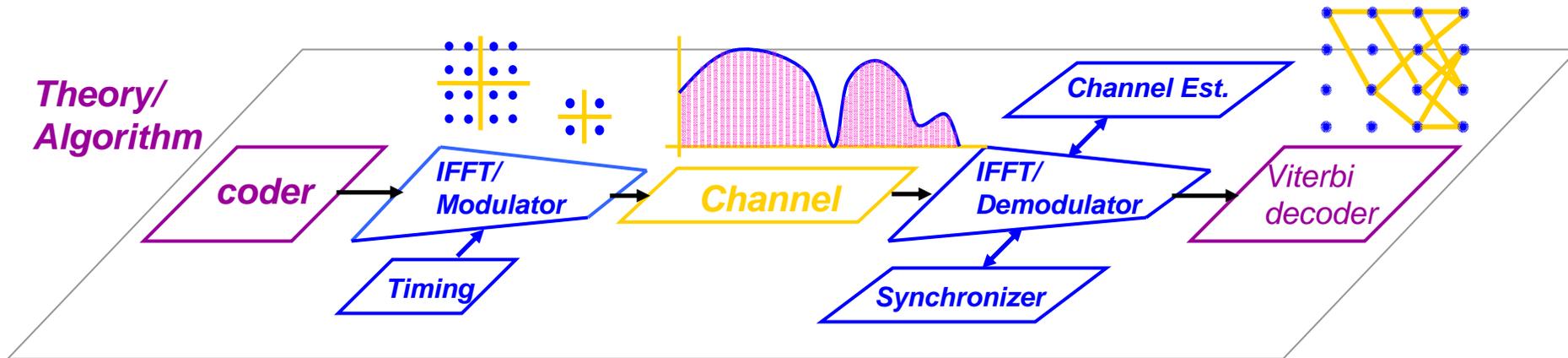


Figure by MIT OpenCourseWare.



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Communication theory view



- ❑ Multitone modulations
- ❑ Convolutional/Block coding and Viterbi/RS decoding
- ❑ Synchronization – tracking loops
- ❑ Channel Estimation

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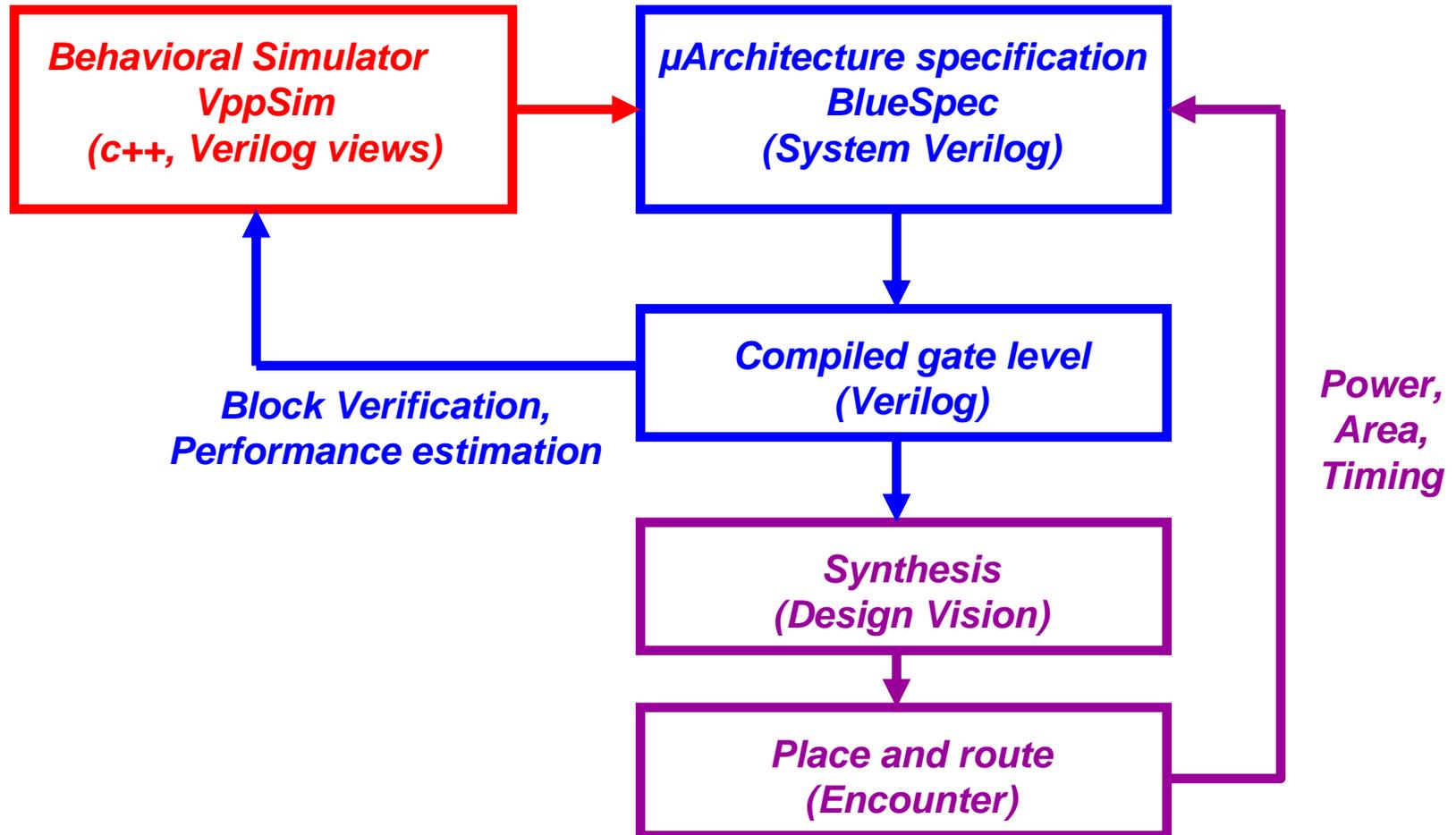
Implementation view - μ Architecture

Image removed due to copyright restrictions.

- FFT
 - Radix 2,4,8
- Viterbi
 - ACS - radix 2,4
 - Traceback vs. Reg. Exch
- Synchronization
 - Correlators
 - CORDIC
 - Tracking loops
- Channel Estimation
 - Equalization
 - Mean-square

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Our ASIC design flow



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VppSim project snapshot

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- ❑ Cadence schematic editor
- ❑ Block modules written in C++ or Verilog
- ❑ Co-simulation C++/Verilog

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Logic synthesis with Design Vision

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Screenshot of "Design View" program.

- ❑ Behavioral to structural RTL
- ❑ Makes Bluespec generated Verilog RTL more compact

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Place and route (Encounter)

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Screenshot of "Encounter" program.

- ❑ Synthesized structural RTL to placed and routed design
- ❑ Get area, power and timing estimates

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Class logistics

□ Lectures

- M,W 1-2:30pm
- Prerequisites: 6.011 and 6.111
- Units: 3-1-8, 6 EDPs (H level)
- Contact:
 - Professor Vladimir Stojanović
 - TA Steven Gerding
- Office hours after the lecture and tutorials

□ Tutorials

- On Fridays 1:00-2:30pm – first six weeks
 - CppSim, Verilog, 802.11a Arch, Bluespec, Design Flow 1 & 2

□ Design lab

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Assignments and grades

- ❑ Exams are take home (little math, mostly Matlab)
 - Exam 1 - 15%
 - Exam 2 - 15%
 - No collaboration
- ❑ Homeworks
 - Three major, 15% each
 - FFT, Viterbi, Synchronization and Channel Estimation
 - Collaboration is o.k. but need to design everything yourself
 - Three minor, 5% each
 - Equalization and multi-tone, 802.11a behavioral, Bluespec
 - No collaboration
- ❑ Final presentation and writeup, 10%

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Similar course is 6.375

- ❑ Uses same tool-flow (Bluespec to gates)
 - Does not use VppSim
 - Have to write your own test harnesses
- ❑ More focused on hardware
 - Doesn't offer the “vertical” view
 - You can choose your own project
- ❑ Not a bad idea to listen to lectures in one or the other course
- ❑ We'll share the lab with 6.375 people
- ❑ Lectures MWF 2:30-4

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6.973 Communication System Design

Recommended readings

- ❑ Posted on the web site (stellar)
- ❑ Recommended books on reserve in Barker
- ❑ Papers
 - 802.11a implementations
 - FFT
 - Viterbi algorithm
 - Convolutional codes and Trellis coded modulation
 - Synchronization
 - Block codes (if time permits)

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For Friday

- ❑ Read the CppSim primer
- ❑ Start reading Chapter 1 in Digital Communications reader posted online
- ❑ CppSim tutorial will be this Friday Feb. 10
- ❑ Tutorials are hands-on
 - Highly advise you attend
 - Will save you a ton of time later