

## 6.777J/2.372J Design and Fabrication of Microelectromechanical Devices Spring Term 2007

Massachusetts Institute of Technology

### In-Class Design Exercise

April 25, 2007

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Accelerometers are starting to be deployed for consumer applications such as cell phones. Accelerometers in this market do not need high precision or accuracy, but they must occupy a small-volume, low-profile package. Below is a simplified schematic for the accelerometer that we will consider in this exercise. You'll later find out that they are fancier than this, but for now, this is quite challenging enough.

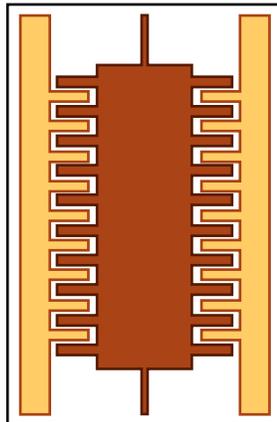


Image by MIT OpenCourseWare.

#### Specifications

- Area of capacitive fingers:  $100,000 \mu\text{m}^2$
- Mass of proof mass:  $3 \mu\text{g}$  ( $\rho_{\text{Si}}=2300 \text{ kg/m}^3$ )
- Max area of system:  $15 \text{ mm}^2$
- Max height:  $2.0 \text{ mm}$
- Number of bond pads: 4
- On-chip bond pad size:  $50 \mu\text{m} \times 50 \mu\text{m}$  (unless using CSP, in which case use those dimensions)
- Spacing between on-chip bond pads:  $50 \mu\text{m}$  (unless using CSP)
- Packaged device must withstand reflow temperatures for flip chip mounting of packaged device.
- Packaged in vacuum.
- Electrical connection from proof mass fingers to 4 bond pads.

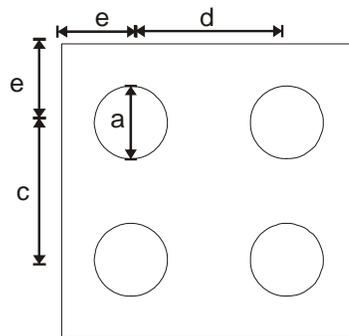
Your task is to design a fabrication process flow and a package process to create an accelerometer that meets the above specs. You should determine the important dimensions of your device and package. You're free to use bulk micromachining or surface micromachining, to start your packaging at the wafer scale or not, etc. You need to consider everything: when the wafer is diced, when the proof mass is released, attachment into the package, etc. Be sure to think about unintended interactions, such as thermal mismatch. Make sure that you meet the specs above; within those constraints, your goal is to come up with the smallest packaged device that can be mounted on a circuit board.

## Packaging options

### Wafer-level chip-scale packaging (CSP)

*Image removed due to copyright restrictions.*

- Hermetic: Dictated by chip.
- Package thickness: Equal to chip thickness + 100  $\mu\text{m}$  for solder bumps.
- Maximum chip thickness: none
- Note: solder bumps are applied at the wafer level. The wafer must be able to withstand electroplating of a 5  $\mu\text{m}$  Cu seed layer onto the pads, screen printing a solder paste, and then reflowing the paste at 225  $^{\circ}\text{C}$  to form bumps.
- Dimensions:

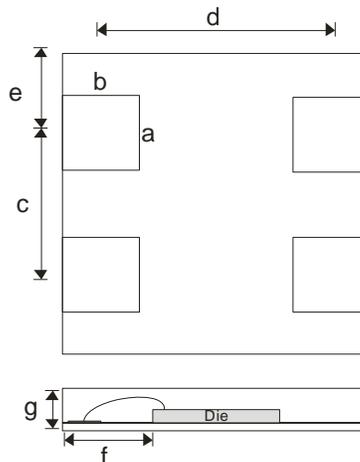


	(mm)
a	0.18
c,d	$\geq 0.5$
e	$\geq 0.32$

### Leadless ceramic chip carrier (LCCC)

*Image removed due to copyright restrictions.*

- Hermetic: Yes.
- Package thickness: 1.8 mm
- Maximum chip thickness: 800  $\mu\text{m}$
- Dimensions:



	(mm)
a	0.64
b	1.27
c,d	$\geq 1.27$
e	$\geq 1.27$
f	1.0
g	1.8

## Dual flat no-lead package (DFN)

*Image removed due to copyright restrictions.*

Hermetic: No.

Package thickness: 0.9 mm

Maximum chip thickness: 350  $\mu\text{m}$

Dimensions:

