

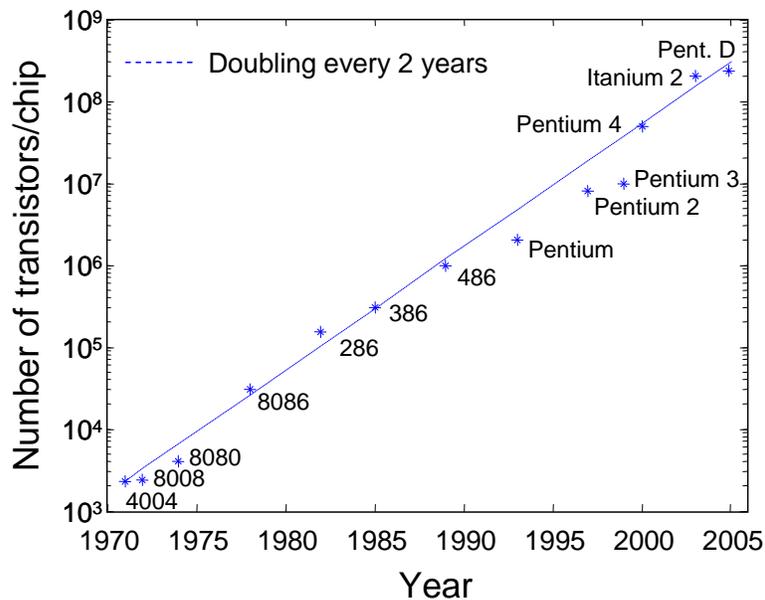
## Introduction

## Introduction

Modern technology is characterized by its emphasis on miniaturization. Perhaps the most striking example is electronics, where remarkable technological progress has come from reductions in the size of transistors, thereby increasing the number of transistors possible per chip.

With more transistors per chip, designers are able to create more sophisticated integrated circuits. Over the last 35 years, engineers have increased the complexity of integrated circuits by more than *five orders of magnitude*. This remarkable achievement has transformed society. Even that most mechanical creature of modern technology, the automobile, now typically contains half its value in electronics.<sup>†</sup>

The industry's history of steady increases in complexity was noted by Gordon Moore, a co-founder of Intel. The eponymous Moore's law states *the complexity of an integrated circuit, with respect to minimum component cost, will double in about 18 months*. Over time the 'law' has held up pretty well; see Fig. 1.



**Fig. 1.** The number of transistors in Intel processors as a function of time. The trend shows a doubling approximately every two years rather than 18 months as originally predicted by Gordon Moore.

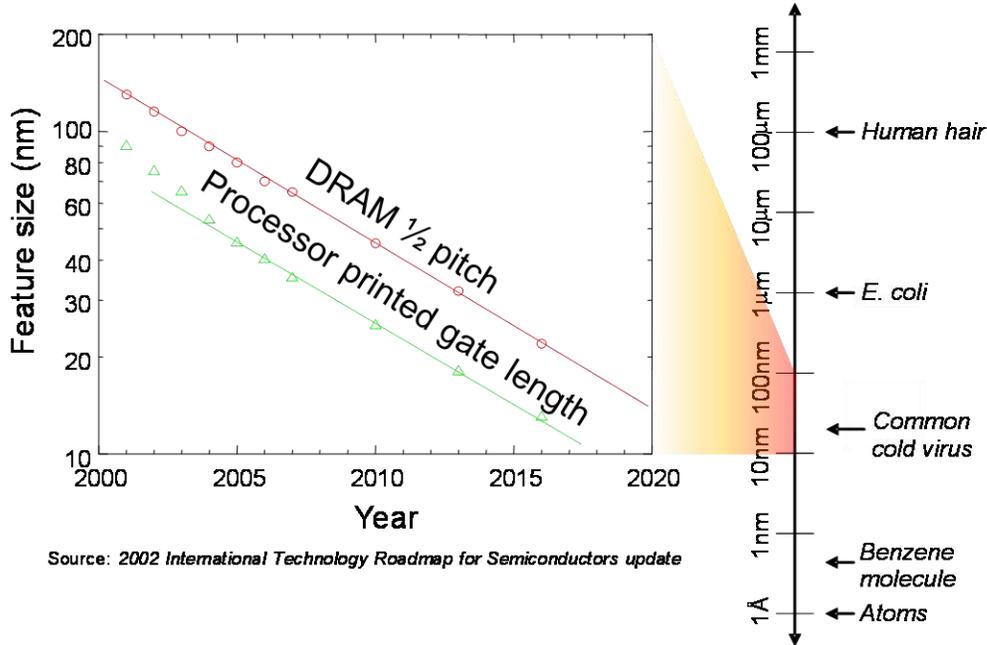
Miniaturization has helped the digital electronics market alone to grow to well over \$300 billion per year. The capital investments required of semiconductor manufacturers are substantial, however, and to help reduce risks, in 1992 the Semiconductor Industries

<sup>†</sup> If this seems hard to believe, consider the number of systems controlled electronically in a modern car. The engine computer, the airbags, the anti-skid brakes, etc..

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Association began the prediction of major trends in the industry – the International Technology Roadmap for Semiconductors – better known simply as ‘the roadmap’.

The roadmap is updated every few years and is often summarized by a semi-log plot of critical feature sizes in electronic components; see Fig. 2.



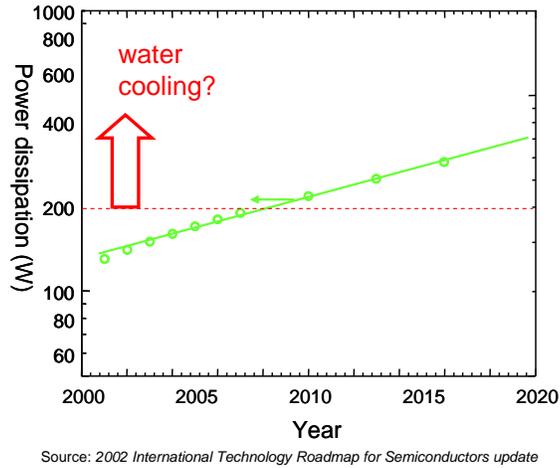
**Fig. 2.** The semiconductor roadmap predicts that feature sizes will approach 10 nm within 10 years. Data is taken from the 2002 International Technology Roadmap for Semiconductors update.

At the time of writing, the current generation of Intel central processing units (CPUs), the Pentium D, has a gate length of 65 nm. According to the roadmap, feature sizes in CPUs are expected to approach molecular scales (< 10 nm) within 10 years.

But exponential trends cannot continue forever.

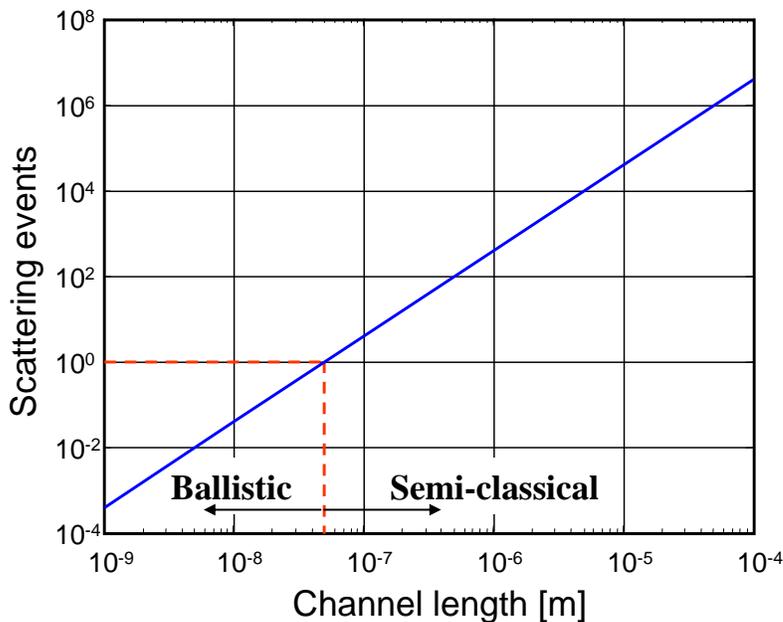
Already, in CPUs there are glimmers of the fundamental barriers that are approaching at smaller length scales. It has become increasingly difficult to dissipate the heat generated by a CPU running at high speed. The more transistors we pack into a chip, the greater the power *density* that we must dissipate. At the time of writing, the power density of modern CPUs is approximately 150 W/cm<sup>2</sup>; see Fig. 3. For perspective, note that the power density at the surface of the sun is approximately 6000 W/cm<sup>2</sup>. The sun radiates this power by heating itself to 6000 K. But we must maintain our CPUs at approximately room temperature. The heat load of CPUs has pushed fan forced convection coolers to the limits of practicality. Beyond air cooling is water cooling, which at greater expense may be capable of removing several hundred Watts from a 1cm<sup>2</sup> sized chip. Beyond water cooling, there is no known solution.

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**Fig. 3.** Expected trends in CPU power dissipation according to the roadmap.

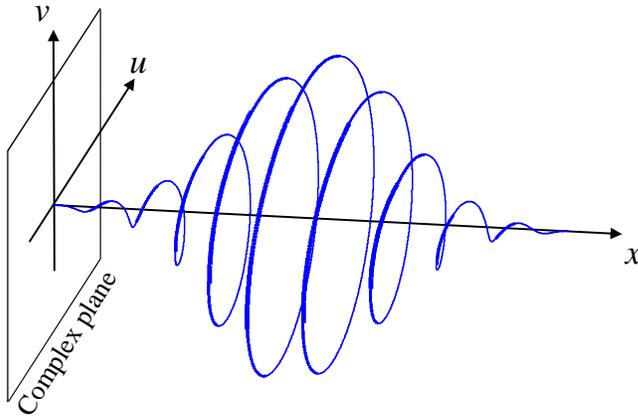
Power dissipation is the most visible problem confronting the electronics industry today. But as electronic devices approach the molecular scale, our traditional understanding of electronic devices will also need revision. Classical models for device behavior must be abandoned. For example, in Fig. 4, we show that many electrons in modern transistors electrons travel ‘ballistically’ – they do not collide with any component of the silicon channel. Such ballistic devices cannot be analyzed using conventional transistor models. To prepare for the next generation of electronic devices, this class teaches the theory of current, voltage and resistance from atoms up.



**Fig. 4.** The expected number of electron scattering events in a silicon field effect transistor as a function of the channel length. The threshold of ballistic operation occurs for channel lengths of approximately 50nm.

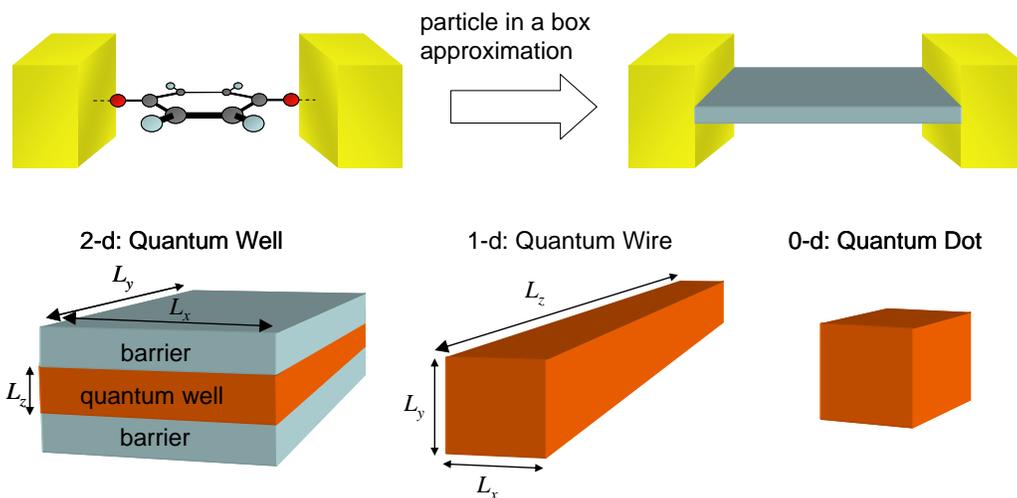
# Introduction to Nanoelectronics

In Part 1, ‘The Quantum Particle’, we will introduce the means to describe electrons in nanodevices. In early transistors, electrons can be treated purely as point particles. But in nanoelectronics the position, energy and momentum of an electron must be described probabilistically. We will also need to consider the wave-like properties of electrons, and we will include phase information in descriptions of the electron; see Fig. 5. The mathematics we will use is similar to what you have already seen in signal processing classes. In this class we will assume knowledge of Fourier transforms.



**Fig. 5.** A representation of an electron known as a wavepacket. The position of the electron is described in 1 dimension, and its probability density is a Gaussian. The complex plane contains the phase information.

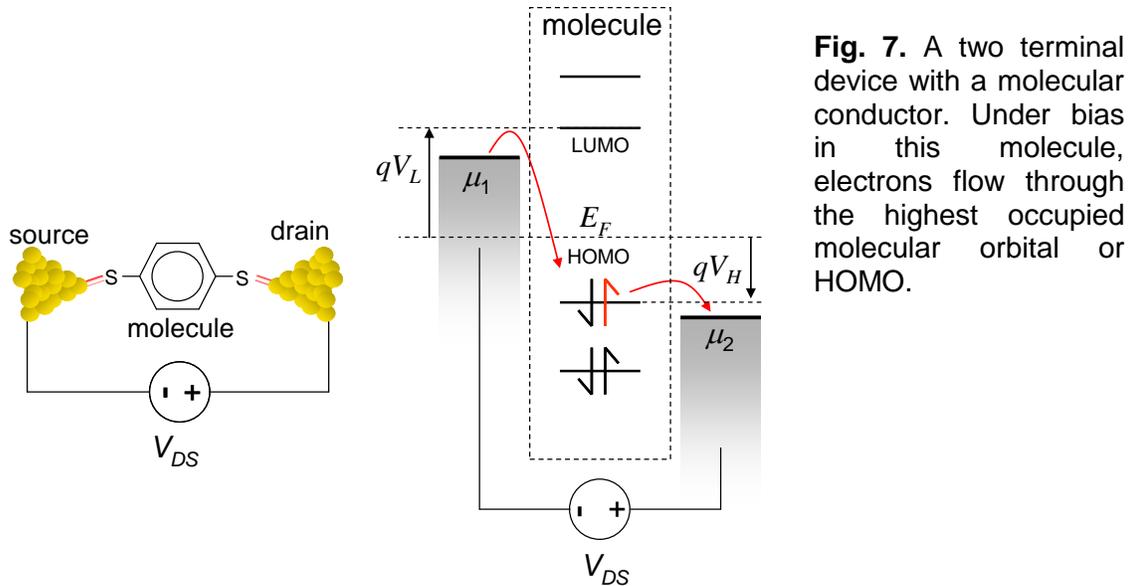
Part 1 will also introduce the basics of Quantum Mechanics. We will solve for the energy of an electron within an attractive box-shaped potential known as a ‘square well’. In Part 2, ‘The Quantum Particle in a Box’, we apply the solution to this square well problem, and introduce the simplest model of an electron in a conductor – the so-called particle in a box model. The conductor is modeled as a homogeneous box. We will also introduce an important concept: the density of states and learn how to count electrons in conductors. We will perform this calculation for ‘quantum dots’, which are point particles also known as 0-dimensional conductors, ‘quantum wires’ which are ideal 1-dimensional conductors, ‘quantum wells’ (2-dimensional conductors) and conventional 3-dimensional bulk materials.



**Fig. 6.** The particle in a box approximation and conductors of different dimensionality.

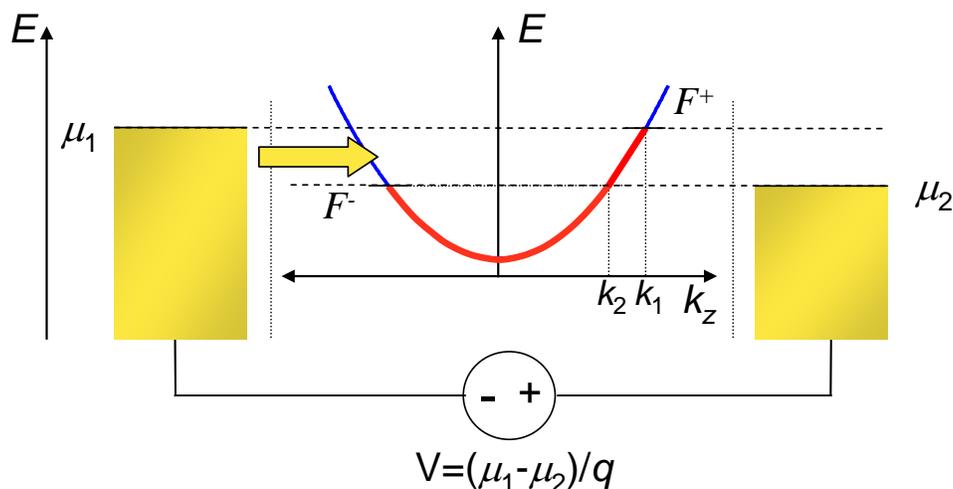
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In Part 3, ‘Two Terminal Quantum Dot Devices’ we will consider current flow through the 0-dimensional conductors. The mathematics that we will use is very simple, but Part 3 provides the foundation for all the description of nano transistors later in the class.



**Fig. 7.** A two terminal device with a molecular conductor. Under bias in this molecule, electrons flow through the highest occupied molecular orbital or HOMO.

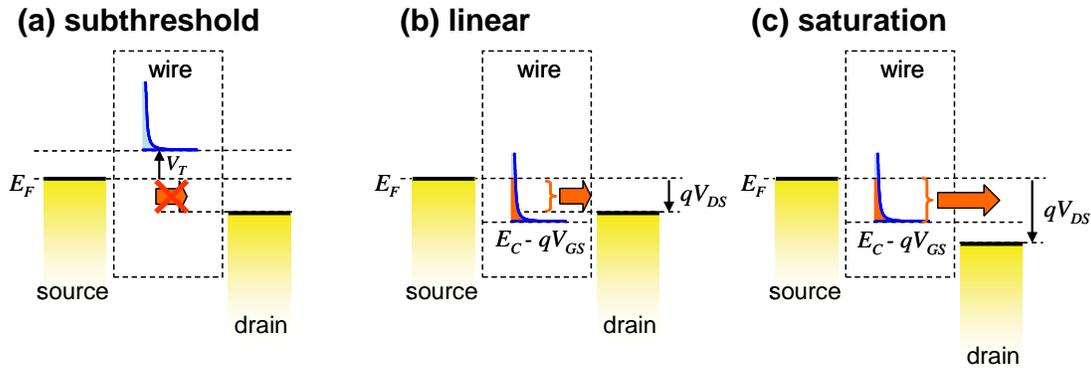
Part 4, ‘Two Terminal Quantum Wire Devices’, explains conduction through nanowires. We will introduce ‘ballistic’ transport – where the electron does not collide with any component of the conductor. At short enough length scales all conduction is ballistic, and the understanding ballistic transport is the key objective of this class. We will demonstrate that for nanowires conduction is quantized. In fact, the resistance of a nanowire of vanishingly small cross section can be no less than 12.9 k $\Omega$ . We will also explain why this resistance is independent of the length of the nanowire! Finally, we will explain the origin of Ohm’s law and ‘classical’ models of charge transport.



**Fig. 8.** From Part 4, this is a diagram explaining charge conduction through a nanowire. The left contact is injecting electrons. The resistance of the wire is calculated to be 12.9 k $\Omega$  independent of the length of the wire.

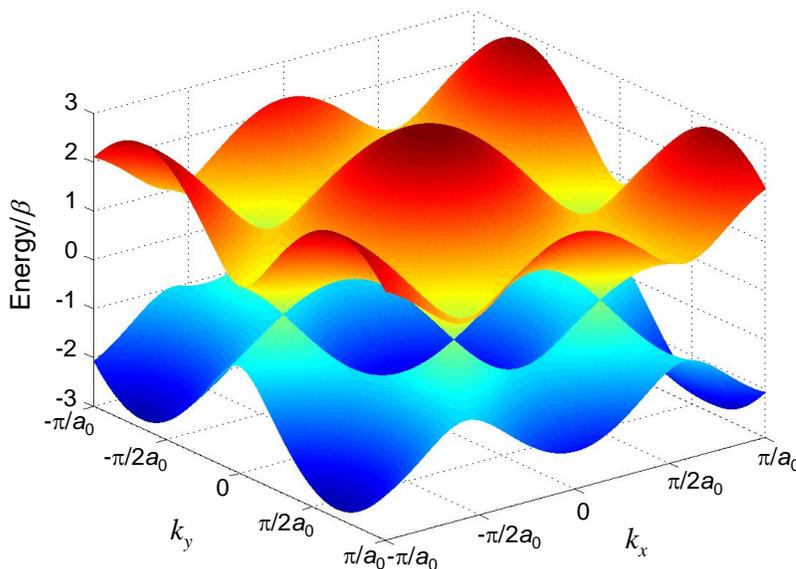
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In Part 5, ‘Field Effect Transistors’ we will develop the theory for this most important application. We will look at transistors of different dimensions and compare the performance of ballistic and conventional field effect transistors. We will demonstrate that conventional models of transistors fail at the nanoscale.



**Fig. 9.** Three modes of operation in a nanowire field effect transistor. In subthreshold only thermally excited electrons from the source can occupy states in the channel. In the linear regime, the number of available states for conduction in the channel increases with source-drain bias. In saturation, the number of available channel states is independent of the source-drain bias, but dependent on the gate bias.

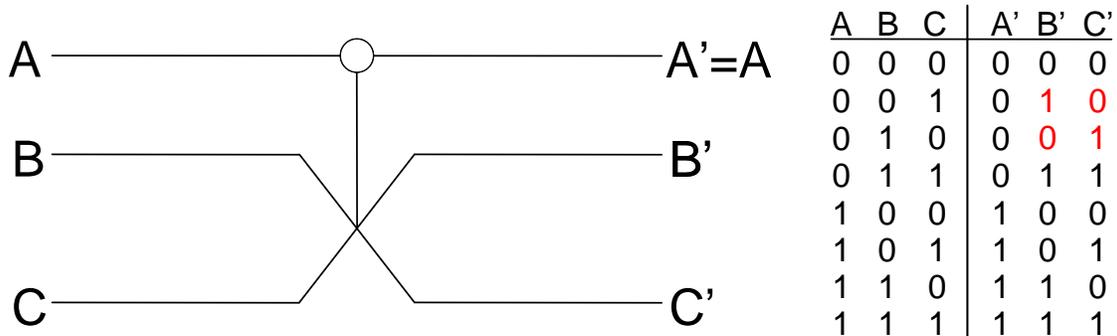
Part 6, ‘The Electronic Structure of Materials’ returns to the problem of calculating the density of states and expands upon the simple particle-in-a-box model. We will consider the electronic properties of single molecules, and periodic materials. Archetypical 1- and 2-dimensional materials will be calculated, including polyacetylene, graphene and carbon nanotubes. Finally, we will explain energy band formation and the origin of metals, insulators and semiconductors.



**Fig. 10.** This is the bandstructure of graphene. There are two surfaces that touch in 6 discrete point corresponding to 3 different electron transport directions within a sheet of graphene. Along these directions graphene behaves like a metal. Along the other conduction directions it behaves as an insulator.

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The class concludes with Part 7, 'Fundamental Limits in Computation'. We will take a step back and consider the big picture of electronics. We will revisit the power dissipation problem, and discuss possible fundamental thermodynamic limits to computation. We will also introduce and briefly analyze concepts for dissipation-less 'reversible' computing.



**Fig. 11.** The Fredkin gate is a reversible logic element which may be used as the building block for arbitrary logic circuits. The signal A may be used to swap signals B and C. Because the input and output of the gate contain the same number of bits, no information is lost, and hence the gate is, in principle, dissipation-less. After Feynman.

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