

# FAQs and Overview of Problem Set 4

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## Notes and Hints:

### Problem 1:

- Q: What is the grid?  
A: Many modern technologies allow you to layout devices with a finer granularity than lambda. The grid value tells you what the granularity is. As the directions state, the dimensions of your devices should be integer multiples of **THE GRID SIZE** (Note: The FAQ had a typo for a while - it said lambda. The pset is correct, and this note has been corrected). DO NOT turn in a width that looks like  $W=1.3532334564355!!!$
- Q: Why does the DUT FET only have  $3*0.7fF$  at the input?  
A: READ THE DIRECTIONS! Every FET has a fanout of 4. The inverter driving the DUT drives  $3*0.7fF$  (modeling 3 inverters) plus the DUT (the fourth inverter).
- Q: I'm using a subcircuit in hspice to model the inverter. How can I measure the drain current,  $I_d$ , on the NMOS device inside the inverter?  
A: You can access nodes inside a subcircuit by using the following notation:  
`.print tran i(xsubcircuitname.mfetname)`  
You can access nodes inside nested subcircuits by using more levels with the '.'
- Q: Is the grid size lambda? Is  $\lambda=0.0025\mu m$ ?  
A: NO!  $\lambda = 0.035\mu m$  because the minimum length is  $0.07\mu m$ .
- Q: What does "Measure leakage for the input that gives the worst-case improvement" mean?  
A: Different inputs to the circuits of interest will produce different leakage currents. You should make your measurements using the input that gives the worst-case improvement. You should be able to predict which input this will be - if not, come to office hours or try them all to see.
- Q: My leakage currents settle slowly! When do I measure the leakage?  
A: Measure leakage current once it has settled. You need to set up your simulation to last long enough to see this occur (\*many\* microseconds). If it is taking forever to run, increase the step size in your .tran statement.
- Q: What  $t_p$  do we use?  $(tpHL+tpLH)/2$  or just the affected transition?  
A: The problem says to use  $t_p$  which we have defined in class as  $(tpHL+tpLH)/2$ .
- Q: In part (c), can we assume a given input?  
A: No. Then you cannot assume anything about the input 'IN'. You may add an

optional 2-input gate, however, and you can connect its second input (IN2) to whatever you wish.

- Q: In table two, should there be separate cases of I\_Base for series and parallel?  
A: Yes. There should be two cases.

#### Problem 2:

- The input vector file has 33 columns

The signals in the columns are:

A[15:0],B[15:0],Cin

- To run SimWave type the following:  
athena\setup synopsys  
synopsys\wd

This will bring up the waveform viewer.

To view your outputs, just load the database of your design. The format that you should use is EPIC and you just need to choose the .out file.

- In order to get the wiring capacitances in your Hspice netlist, when extracting from Magic you should use the following command at the Athena prompt.

```
ext2spice -o file_name.sp file_name.ext -c 0
```

- The SUM outputs and the last COUT output should have an additional load of 30fF.  
Add it manually in your spice deck.
- If you don't have access to a color printer, you can print your design the athena color printer located in the Copy Tech, at the student center
- The power can be found by adding 'report\_block\_powr total \*' as an additional line in your cfg file.