

6.374: Analysis and Design of Digital Integrated Circuits
Problem Set # 4

Fall 2003

Issued: 10/14/03

Due: 10/28/03

Problem 1: MTCMOS Sleep Device Sizing

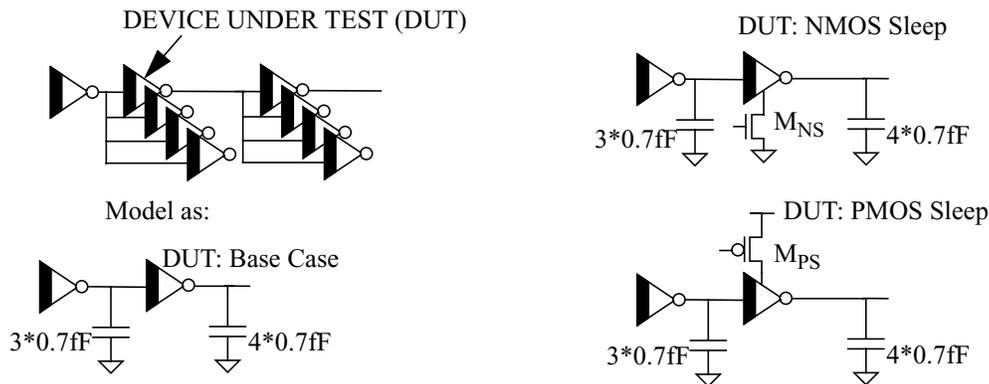


Figure 1: A driver circuit schematic

This problem examines sizing for MTCMOS sleep devices in a cutting edge technology. The devices in the problem are $0.07\mu\text{m}$ FETs modeled by a Predictive BSIM model. We generated the predicted models using Berkeley Predictive Technology Model (<http://www-device.eecs.berkeley.edu/~ptm/introduction.html>). You may find this site useful for generating models to use in your project.

Please use the following assumptions in this problem:

- Every inverter has a fanout of 4. The gate capacitance of an inverter can be approximated as $0.7\text{fF}/\text{FET}$.
- All LVT inverters have PMOS $W/L = 0.22\mu\text{m}/0.07\mu\text{m}$ and NMOS $W/L = 0.1\mu\text{m}/0.07\mu\text{m}$.
- $V_{DD} = 1.2\text{V}$.
- $AS = AD = 6 * \lambda * W$ and $PS = PD = 10 * \lambda + W$.
- The minimum grid size is $0.0025\mu\text{m}$. In other words, the width of your FETs should be $N * 0.0025\mu\text{m}$, $N = \text{integer}$.
- To get the model files, type the following four lines in HSPICE deck:


```
.include 'nfet007hvt.l'
.include 'nfet007lvt.l'
.include 'pfet007hvt.l'
.include 'pfet007lvt.l'
```
- To instantiate a FET, use the following names: NMOShvt, NMOSlvt, PMOShvt, PMOSlvt.
- When finding leakage, assume $V_{GS} = 0$. Measure leakage for the input that gives the worst-case improvement.
- HINT: Use subcircuits to make your life easier. The documentation on the webpage shows how.
- HINT: To simulate settling leakage currents, add the following lines to your HSPICE deck:


```
.options accurate
.options method=gear
```

a) For the circuits in Figure 1, use HSPICE to find a size for M_{NS} and another for M_{PS} such that the inverters only see

10% reduction in propagation delay. Repeat your simulation to find sizes to achieve only 5% degradation in t_p . Turn in ONLY the following:

i) Fill out Table 1.

ii) Transient simulation plot showing I_D settle to the sleep value when the inverter enters sleep mode. Use the drain current in the NMOS device in the inverter for your measurements. Show the current settling for all four cases on one plot (PMOS 5%, PMOS 10%, NMOS 5%, NMOS 10%). Use a SEMILOG plot (Y-axis log).

Table 1: Results from Part (a)

Delay Penalty	M_{NS} (um)	M_{PS} (um)	I_{DBASE} (nA)	I_{DNS} (nA)	I_{DPS} (nA)	I_{DBASE}/I_{DNS} (X)	I_{DBASE}/I_{DPS} (X)
5%							
10%							

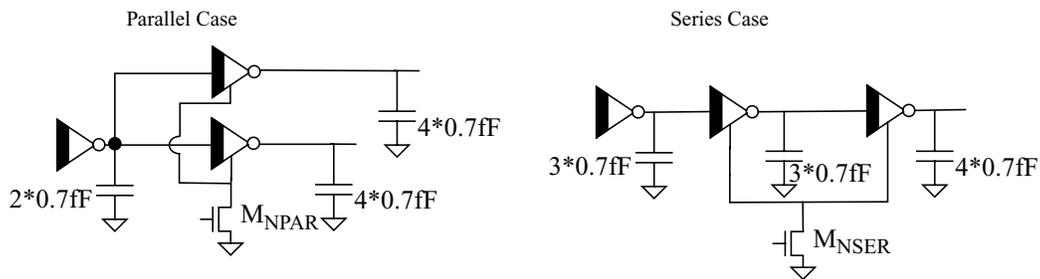


Figure 2: Sizing Sleep Devices for Parallel and Series Inverters

b) Refer to Figure 2. Use HSPICE to size M_{NSER} and M_{NPAR} for both cases to achieve 5% and 10% delay degradation over the *appropriate* base case. Turn in ONLY the following:

i) Fill out Table 2.

Table 2: Results from Part (b)

Delay Penalty	Parallel M_{NPAR} (um)	Series M_{NSER} (um)	I_{DBASE} (nA)	I_{DSER} (nA)	I_{DPAR} (nA)	I_{DBASE}/I_{DSER} (X)	I_{DBASE}/I_{DPER} (X)
5%							
10%							

c) Refer to Figure 3. Try to minimize standby leakage current. You may use any number of sleep devices with or without sharing. You also may insert a 2-input gate into the dotted box. Use HSPICE to minimize standby leakage current while maintaining no more than a 10% delay penalty. Turn in ONLY the following:

i) A schematic of the circuit including the sleep devices and their sizes.

ii) The total width of the sleep devices.

iii) The total leakage savings in standby mode relative to active mode leakage (in X, for worst-case).

iv) A transient simulation showing the total leakage current settling to its steady-state value when the circuit enters sleep. Use a SEMILOG plot (Y-axis).

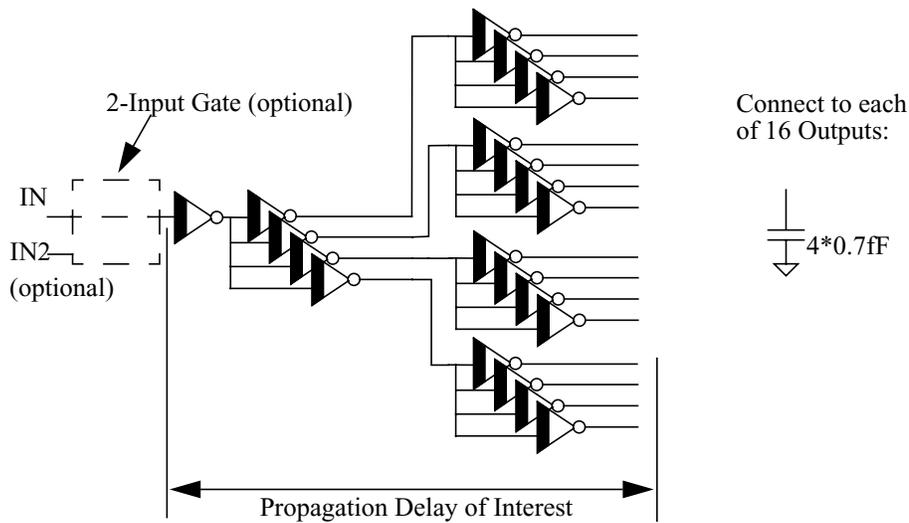


Figure 3: Sizing Sleep Device(s) for an Inverter Tree

Problem 2: Adder Design

You are to design, layout, and simulate an **16-bit ripple carry adder** with the following specifications:

Table 3: Input/Output Signals

Input	Description	Output	Description
A[15:0]	15-bit operand	S[15:0]	15-bit output sum vector
B[15:0]	15-bit operand	Co	Carry out
Ci	Carry in		

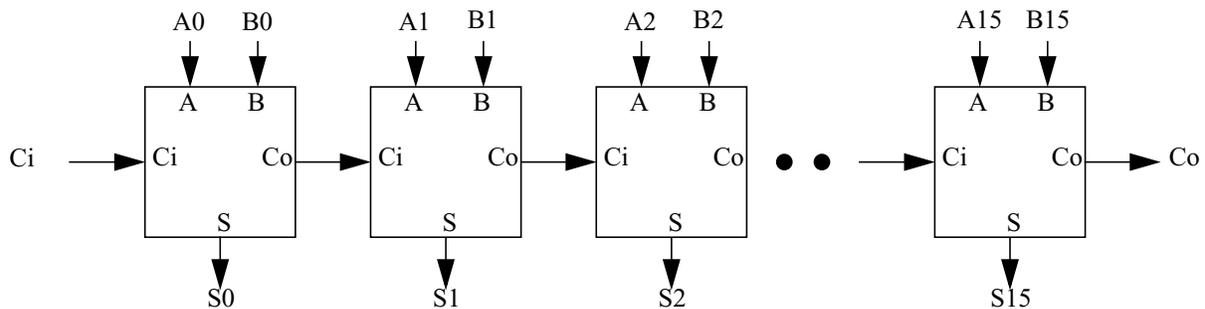


Figure 4: 16-bit ripple carry adder

Your inputs have to go through two minimum length inverters ($W_p/W_n=1.125/0.375$) before driving the adder inputs in your netlist (do **NOT** layout these inverters). All outputs have a capacitive load of 30fF.

- Layout the adder in MAGIC using **ANY** static CMOS logic style with rail to rail outputs.

Your goal is to **minimize energy/addition** meeting a specific delay constraint, by lowering V_{dd} and/or by your choice of static circuit style. The worst case critical path delay must be $t_p \leq 4ns$. Observe good layout techniques that reduce parasitic capacitances and resistances. Turn in **ONLY**:

- i) a schematic of your 1-bit adder implementation
- ii) the layout of the 1-bit adder and its area
- iii) the layout of the full 16-bit adder and its area

After problem set 2 you have become experts in layout, so your layout should be compact and not excessively spread out. This time there will be points off for unnecessary wasted area (money).

You must print a **color** version of your layout.

- b) Extract and verify that your adder works. You have to use the input vector file located in: *input.vec*. Use SimWave to view your nanosim waveforms. (see FAQ for details). Does your adder work? (Yes/No).
- c) Determine the critical path in the circuit (tell us the input vectors that give the worst case delay), and simulate the extracted circuit in HSPICE with the input pattern displaying the critical path. Turn in a plot showing the worst case propagation delay of your adder.
- d) Using the input vector file located in: *input.vec*, report the dissipated power at $V_{dd}=2.5V$, when the input frequency is 100Mhz. What is the average energy per addition?
- e) Using the input vector file located in: *input.vec*, report the dissipated power at your desired power supply voltage, when the input frequency is 100Mhz. Your design must meet the delay constraint ($t_p \leq 4ns$), at this operating voltage (see part(c)). What is the average energy per addition?

Layout Requirements

All A,B inputs should come in from the top of the cell in metal 1 or 2. All S outputs should come out from the bottom of the cell in metal 1 or 2.

Useful hints and suggestions :

- To find out your plot area in MAGIC use macro 'f' followed by 'b'. This selects your cell and 'boxes' it. You should get the area of the box in terms of your grid size.
- Remember device sizes in Magic are multiples of lamda