

6.374: Analysis and Design of Digital Integrated Circuits
Problem Set # 2 Solutions

Fall 2003

Issued: 9/18/03

Due: 9/30/03

For these problems you should use the parameters for the 0.25 technology (given in the text) unless otherwise specified for a particular problem.

Problem 1: Subthreshold Inverter Operation

In circuit applications where extremely low power consumption is essential and high speed operation is not required, subthreshold logic may provide an ideal solution. This problem will explore how far the supply voltage may be lowered before a CMOS inverter fails. For the entire problem, assume that the both devices are minimum length and that the NMOS device has a width of 0.44 μm . Failure is defined as the point where an input swing of 0 to VDD produces an output swing less than 10% to 90% of VDD. For this problem use the 0.18 micron technology file which is located in “/mit/6.374/models/log018_1.l”. (Research by Alice Wang)

- a) Consider the case where the input to the inverter is 0 V. Will the output voltage remain equal to the supply voltage as the supply voltage is lowered to arbitrarily low values? If not, explain what will happen and why. Would using a wider PMOS device increase or decrease the minimum possible supply voltage? Which process corner (TT, FF, SS, SF, or FS) will be the worst case and why? (Variable process conditions may result in a case where the NMOS and PMOS devices have modified mobilities. TT is the case where both devices are typical, SF has slow NMOS and fast PMOS, etc...)

Solution

When the input is 0 V, V_{gs} for the NMOS device is 0V and V_{gs} for the PMOS is $-V_{DD}$. For typical supply voltages, the current through the PMOS in this case dominates and the output is pulled to V_{DD} . As VDD falls to lower voltages, eventually pushing the PMOS into subthreshold the currents will eventually begin to approach comparable levels and the simple CMOS inverter will become a ratioed circuit. Using a wider PMOS would decrease the minimum possible supply voltage since this would increase the strength of the PMOS relative to the NMOS and allow the PMOS current to overpower the NMOS for lower supply voltages. FS would be the worst case process corner, since the PMOS is weakened in comparison to the NMOS and loses some ability to pull up the output node. So, for a given supply voltage there is a minimum width requirement on the PMOS to maintain proper operation and the minimum size is largest for the FS corner.

- b) Consider the case where the input to the inverter is VDD. Would using a wider PMOS increase or decrease the minimum supply voltage in this case? Which process corner will be the worst case and why?

Solution

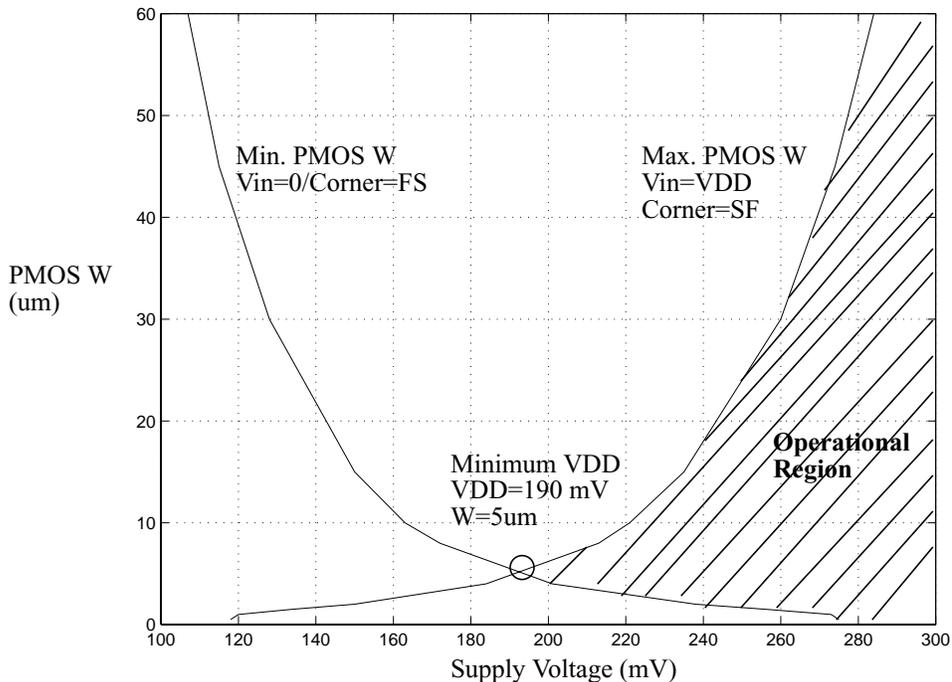
In this case, V_{gs} for the PMOS is 0 V and V_{gs} for the NMOS is lowered with supply voltage. Using a wider

PMOS would increase the minimum supply voltage since the PMOS would be stronger and have more leakage current to pull the output up from its desired value of 0 V. The worst case corner would be SF since this would also increase the output voltage for a given supply voltage. So for a given supply voltage, there is a maximum width for the PMOS to maintain proper operation and the maximum width is smallest for the SF corner. Comparing the results for parts a and b, it is clear that since one case requires large PMOS and one case requires small PMOS there must be an optimum PMOS size to operate at the lowest possible supply voltage.

- c) Now, use HSPICE to simulate the inverter and find the lowest possible supply voltage. Complete one simulation for each input value using the process corners you chose in parts a and b. Use a .DATA statement to vary the width of the PMOS device across the set {0.5u, 1u, 1.5u, 2u, 4u, 8u, 10u, 15u, 30u, 45u, 60u} and sweep VDD from 100mV to 400 mV. Then, using the expressions function in AWaves, plot the ratio of V(out)/VDD. The points where the ratio crosses 0.1 and 0.9 are the failure points. Create a table with three columns containing: PMOS width, minimum supply voltage for the case where the input voltage equals 0, and minimum supply voltage for the case where the input voltage equals VDD.

PMOS Width	0.5u	1.0u	1.5u	2u	4u	8u	10u	15u	30u	45u	60u
Min. VDD (Vin=VDD)	118m	120m	134m	150m	184m	213m	221m	235m	260m	274m	284m
Min. VDD (Vin=0)	275m	273m	256m	238m	201m	172m	163m	150m	128m	115m	107m

- d) Now use your favorite graphing program (Matlab, Excel, etc....) to create a graphical representation for the functional region of operation. On a single graph, plot both cases of (minimum supply voltage, PMOS width) and indicate the region where both conditions are met. What is the lowest possible supply voltage that meets both conditions? What must the PMOS width be to operate at this supply voltage? The minimum supply voltage is about 190 mV and the PMOS must be about 5 um.



Problem 2: CMOS Logic

Consider the following CMOS logic circuits:

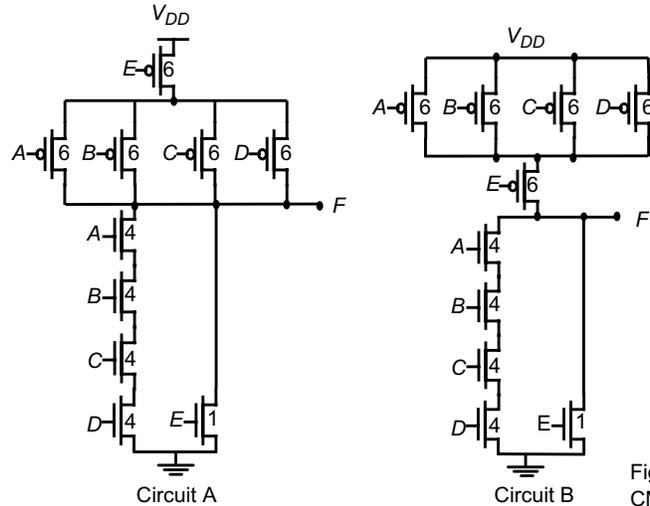


Figure 0.1: Two static CMOS gates.

- a) Do the two circuits in Figure 0.1 implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

Solution

Yes, they implement the same logic function : $F = \overline{(ABCD + E)} = (\overline{A} + \overline{B} + \overline{C} + \overline{D})\overline{E}$

- b) Assuming we can ignore all second order effects, do these two circuits have the same output resistances when driven with the same input patterns?

Solution

Yes, they do. The pull down networks are identical and the pull up network can be found by inspection to have the same resistances given the same input pattern.

- c) Assume the transistors have been sized to give a worst case output resistance of $13 \text{ k}\Omega$ for the worst-case input pattern. What input patterns ($A-E$) give the lowest output resistance when the output is low? What is the value of that resistance?

Solution

The lowest output resistance is obtained when all inputs (A, B, C, D and E) are equal to 1. In that case, the output resistance is the parallel of the resistance of a NMOS of width 1, with a series of four equal nMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, $13 \text{ k}\Omega$. Then the output resistance, in this case, is half this value, $6.5 \text{ k}\Omega$.

- d) What input patterns ($A-E$) give the lowest output resistance when the output is high? What is the value of that resistance?

Solution

The lowest output resistance is obtained when all inputs are equal to zero. Each of the PMOS have the same width, so all of them have the same resistance. The worst case resistance happens when only one of the inputs (A, B, C or D) is equal to 0 while all the rest are equal to 1. The output resistance in that case is the series of the resistance of two of the PMOS and it is equal to $13 \text{ k}\Omega$. Then, each of the pMOS has an output resistance equal to $6.5 \text{ k}\Omega$. The output resistance is equal to the series of one of these resistance with the parallel of four of the same resistances. Then, the minimum output resistance is $6.5 \text{ k}\Omega + 6.5 \text{ k}\Omega / 4 = 8.125 \text{ k}\Omega$.

- e) Neglecting parasitics and assuming a load capacitance of 100 fF , find the best case and worst case t_{plh} and t_{phl} .

Solution

We can use the RC time constant method of $t = 0.69 * R_{\text{eq}} * C_L$. For the worst case, $R = 13 \text{ K}$ for both pull-up and pull-down and the t_{plh} and t_{phl} are both equal to 0.9 ns . For the best case t_{phl} we know that $R = 6.5 \text{ K}$ so $t_{\text{phl}} = 0.45 \text{ ns}$. For the best case t_{plh} we know that $R = 8.125 \text{ K}$ so $t_{\text{plh}} = 0.56 \text{ ns}$.

- f) Now consider a few second order effects on the propagation delays. Which circuit is optimized for the case when it is known a priori that E will be the last input to arrive and why? How will body effect influence the performance of Circuit A vs. Circuit B?

Solution

Circuit B is optimized for the case when 'E' will arrive last. The only difference between the two circuits is the pull up network. The nodes between (ABCD) and (E) can use the time before E arrives to charge up to VDD therefore reducing the time required for the overall circuit to charge after E does arrive. Circuit B is also preferable due to the lower influence of body effect. All four parallel devices in Circuit A may experience an increase in threshold voltage and consequent decrease in drive strength due to body effect.

- g) For parts g and h, consider only Circuit B. Each intermediate node has some parasitic capacitance that must be charged and discharged at each transition. Therefore, the propagation delay is a function of both the initial voltage conditions on the internal nodes and the inputs. The initial voltage conditions, however, are determined by the previous inputs. Which set of previous and current inputs will cause the slowest t_{plh} ? Which will cause the slowest t_{phl} ?

Solution

For the worst case low-to-high output transition, all internal caps should initially be discharged to ground which gives a worst case previous input of $[\text{ABCDE}] = [11110]$. Then, the following input should leave all of those capacitances exposed to the output node so $[\text{ABCDE}] = [11100]$. For the high-to-low transition, we should have $[\text{ABCDE}] = [11100]$ as the previous input to charge up the internal nodes, then $[\text{ABCDE}] = [11110]$ to discharge through a single path only.

- h) Let all devices be minimum length and set the widths according to the relative scale in the diagram with $1 = 0.375 \text{ }\mu\text{m}$, specify your source and drain areas and perimeters, and include an additional 10 fF load. Use Nansim to verify functionality by creating an input file which tests the following set of inputs $[\text{ABCDE}] = [00000, 00001, 11110, 11100, 11111]$. Verify that your simulated output values match the expected logic function. Submit your Nansim output file.

Solution

Your output file should show that, for the input list above, the output should be [OUT]=[1, 0, 0, 1, 0]

Problem 3: Pseudo-NMOS Logic

Consider the circuit of Figure 0.2.

- a) What is the output voltage if only one input is high? If all four inputs are high?

Solution

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

Consider a case when one input is high: $A = V_{DD}$ and $B = C = D = 0$ V. Assume that V_{out} is small enough that $V_{min} = V_{DSAT}$ for the PMOS device, and $V_{min} = V_{DS} = V_{out}$ for the NMOS devices. Solve for V_{out} by setting the drain currents in the PMOS and NMOS equal to each other, $|I_{DP}| = |I_{DN}|$, where the drain currents are functions of V_{out} , V_{DD} , and the device parameters.

$$V_{out} = 102 \text{ mV}, \text{ and } I_D = 35.7 \text{ } \mu\text{A}.$$

Now verify that the assumptions for V_{min} are correct. For the PMOS: $V_{DS} = -2.34$ V, $V_{DSAT} = -1$ V, $V_{GT} = -2.1$ V, therefore $V_{min} = V_{DSAT}$. For the NMOS: $V_{DS} = 102$ mV, $V_{DSAT} = 630$ mV, $V_{GT} = 2.07$ V, therefore $V_{min} = V_{DS}$.

Consider the case when all inputs are high: $A = B = C = D = V_{DD}$. For these hand calculations, this is numerically equivalent to a circuit with a single NMOS device with $W/L = 4 * 1.5$ and its gate tied to V_{DD} . Now, the analysis used above for the case when one device is on can be reused, replacing W/L of the NMOS with 6, and using the same assumptions for V_{min} . $V_{out} = 25$ mV, and $I_D = 35.9 \text{ } \mu\text{A}$. The assumptions for V_{min} are correct.

- b) What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

Solution

Notice in part a) that the drain current in the PMOS is $35.7 \text{ } \mu\text{A}$ with one NMOS on and $35.9 \text{ } \mu\text{A}$ with four NMOS devices on. The current in the PMOS can be approximated as $35.8 \text{ } \mu\text{A}$ when any number of NMOS devices are on and $0 \text{ } \mu\text{A}$ when all four are off. The probability that all four NMOS devices are off is $(1-p)^4$ where p is the probability an input is high. Therefore,

$$P_{AVG} = P_{OFF} \cdot (1-p)^4 + P_{ON} \cdot [1 - (1-p)^4]$$

where $P_{OFF} = 0$ W, and $P_{ON} = 89.5 \text{ } \mu\text{W}$. $P_{AVG} = 83.9 \text{ } \mu\text{W}$ when $p = 0.5$ and $P_{AVG} = 30.7 \text{ } \mu\text{W}$ when $p = 0.1$.

- c) Compare your analytically obtained results to a SPICE simulation.

Solution

From SPICE: $V_{out} = 98.7$ mV, and $I_D = 38.2 \text{ } \mu\text{A}$ with one NMOS device on and $V_{out} = 23.5$ mV, and $I_D =$

38.3 μA with all NMOS devices on

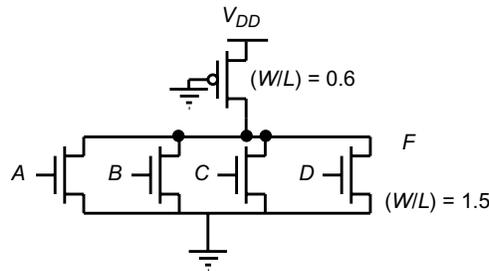
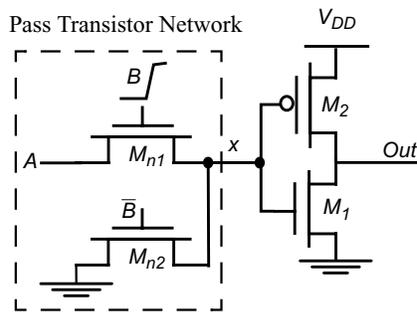


Figure 0.2 Pseudo-NMOS gate.

Problem 4: Pass Transistor Logic and Level Restoration

Consider the circuit of Figure 0.3. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.



$$\begin{aligned}
 V_{DD} &= 2.5\text{V} \\
 (W/L)_2 &= 1.5\mu\text{m}/0.25\mu\text{m} \\
 (W/L)_1 &= 0.5\mu\text{m}/0.25\mu\text{m} \\
 (W/L)_{ni} &= 0.5\mu\text{m}/0.25\mu\text{m} \\
 k_n' &= 115\mu\text{A}/\text{V}^2, k_p' = -30\mu\text{A}/\text{V}^2 \\
 V_{tN} &= 0.43\text{V}, V_{tP} = -0.4\text{V}
 \end{aligned}$$

Figure 0.3 Level restoring circuit.

- a) What is the logic function performed by this circuit?

Solution

The circuit is a NAND gate.

- b) Explain why this circuit has non-zero static dissipation.

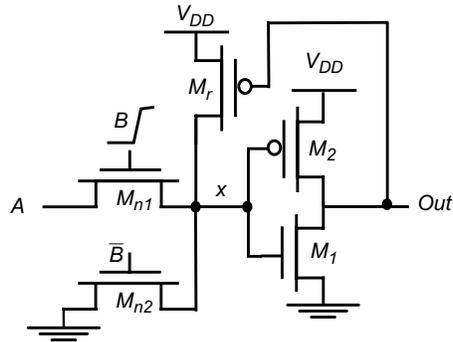
Solution

When $A=B=V_{DD}$, the voltage at node x is $V_X = V_{DD} - V_{tN}$. This causes static power dissipation at the inverter the pass transistor network is driving.

- c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

Solution

The modified circuit is shown in the next figure

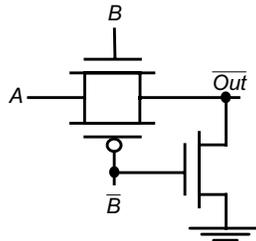


The size of M_r should be chosen so that when one of the inputs A or B equals 0, either M_{n1} or M_{n2} , would be able to pull node X to $V_{DD}/2$ or less.

d) Implement the same circuit using transmission gates.

Solution

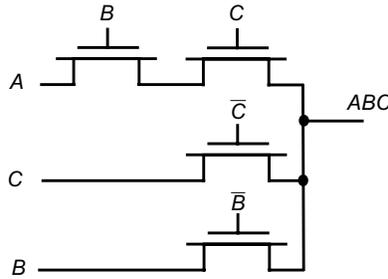
The circuit is shown below.



e) Replace the pass-transistor network in Figure 0.3 with a pass transistor network that computes the following function: $x = ABC$ at the node x. Assume you have the true and complementary versions of the three inputs A,B and C.

Solution

One possible implementation is shown:



Problem 5: Device Modeling - DIBL

The standard equation for modeling subthreshold leakage current given in the notes is

$$I_d = I_o \cdot e^{\frac{V_{GS} - V_T}{nV_{th}}} \cdot \left(1 - e^{\frac{-V_{DS}}{V_{th}}} \right) .$$

This equation does not account for higher order effects like DIBL. The following BSIM equation adds the DIBL effect to the model:

$$I_d = I_o \cdot e^{\frac{V_{GS} - V_{To} - (\gamma' \cdot V_{SB}) + \eta \cdot V_{DS}}{nV_{th}}} \cdot \left(1 - e^{\frac{-V_{DS}}{V_{th}}} \right) .$$

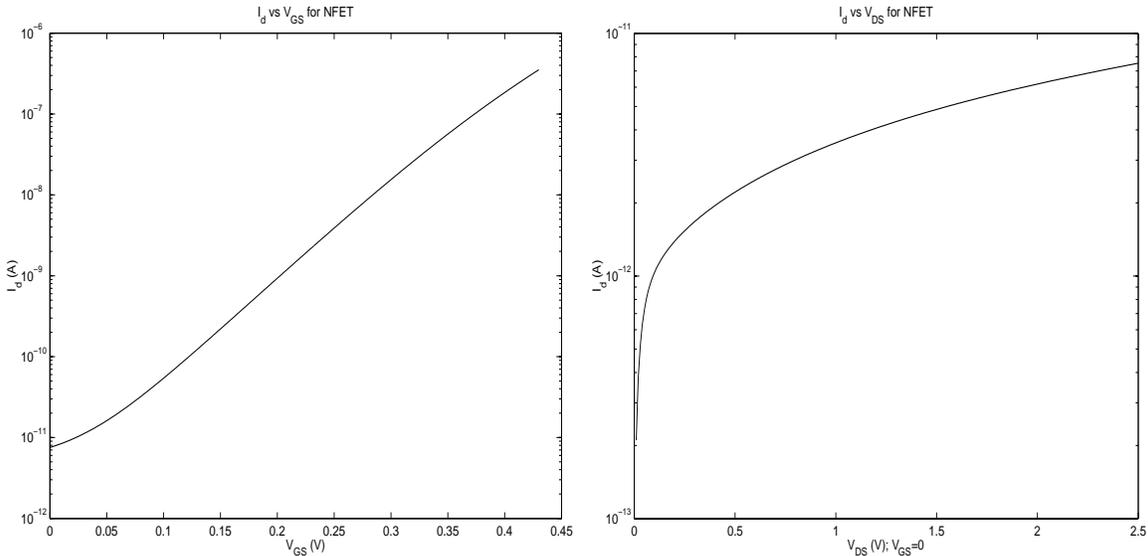
Using this new equation, we will produce a model for the subthreshold leakage in the 0.25µm process used in 6.374.

a) Using HSPICE, plot I_d vs V_{GS} for a single NMOS device with $V_D = V_{DD} = 2.5V$ and $W/L = 0.5\mu m/0.25\mu m$. We are only interested in the subthreshold region, so sweep V_{GS} over the appropriate range.

Using HSPICE, plot I_d vs V_{DS} for $V_{GS}=0V$ over the full range of V_{DS} . Plot the current on a log scale for both plots.

You will need to extract the points along these curves to use in your favorite analysis program (ie Matlab) for the rest of this problem. The following statement in HSPICE prints a table of the sweeping value and the current through a MOSFET to the HSPICE output stream: `.print dc i(Mn1)`

SOLUTION:



Plots of simulated subthreshold current vs V_{GS} and vs V_{DS}.

b) Using the data from the I₀ vs V_{GS} plot, extract a value for S, the subthreshold slope, in mV/decade. Plot S as it varies with V_{GS}. Over which range of V_{GS} is S likely to be the most accurate for modeling? Plot “instantaneous n” as it varies with S. Over which range is it likely to be accurate for modeling?

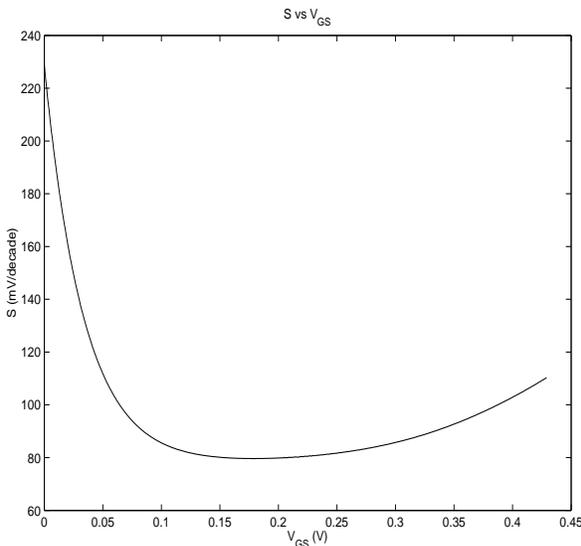
SOLUTION:

The slope of the curve in the I_d vs V_{GS} plot is 1/S. To find S, we need to find the slope of the curve and then take its inverse. We cannot calculate the derivative directly because we want S to be in units of mV/decade. Thus we take the log of the current before finding the slope (notice that we can plot the log₁₀(I_d) vs V_{GS} on a linear scale and get the same shape curve as in the simulation plot above). The following expression then gives the subthreshold slope in mV/decade:

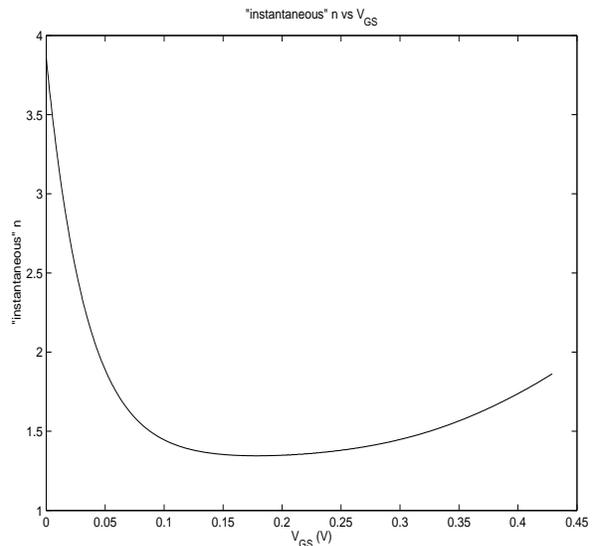
$$S = \frac{\Delta V}{\Delta \log(I_d)}$$

In Matlab, this might look like: S = delV./diff(log10(Id));

where delV is the voltage step in mV. We can solve for “instantaneous n” using S=nV_{th}ln(10). The plots for S and “instantaneous” n appear on the following page. The region of interest is clearly the right side of the graph (V_{GS} about 0.15V and above). The rise in S at low voltages comes from the tail-up of current. This increase in current at low V_{GS} and high V_{DS} results from the GIDL effect (Gate Induced Diode Leakage). For modeling purposes, we will select a value of S and n from the regions of the plots where the slope is more constant.



Plot of S vs V_{GS} .



Plot of "instantaneous n" vs V_{GS} .

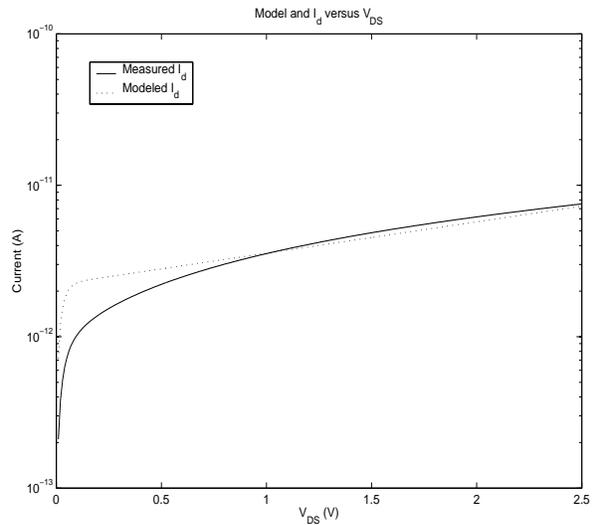
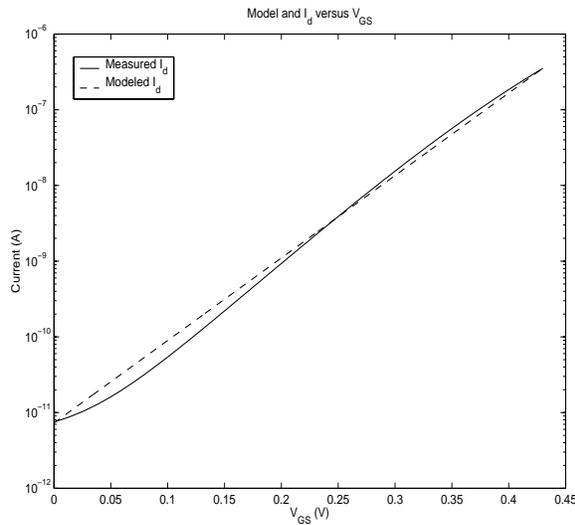
c) Now we will construct a model for the subthreshold behavior of the FET using the BSIM equation. This model should accurately represent the behavior of the FET that you saw in part a). The BSIM equation still is a reasonably low order model, so do not expect your final result to match the plots precisely - just try for a ballpark match. To develop the model, you need to select three parameters: n , I_o , and η . The value for n should be somewhere in the range that you plotted in b). Select I_o so that the drain current supplied by the model matches the simulated value at $V_{GS}=V_{T0}$.

Hints: Pick an initial value for η and use it with your estimates for n and I_o in the model equation for varying V_{DS} . η controls the slope of the curve versus V_{DS} . Once the slopes are roughly equivalent, use your estimate of η to find the current while sweeping V_{GS} . Select values of n and I_o that give a good fit. Now use those values in the other case to refine your choice of η . Iterate this process a few times until you are satisfied with the models. It is helpful to convince yourself (by experimentation or from the equation) of the effects of the different parameters on the current. Remember, there is a range of "right" answers to this part of the problem. Also, be glad you don't do this for a living :)

Turn in a plot of I_o vs V_{GS} with the real data and the model data on the same plot. Do the same for I_o vs V_{DS} . What were your values for I_o , n , and η ? Comment **briefly** on what you consider to be a "good" fit using this model for this process (ie - is it more important to get the slope right or the actual values? is it better to overestimate or underestimate the current? etc). Why is your model a good choice?

We selected $n = 1.55$, $\eta = 0.019$, and $I_o = 1.0715E-7A$. The choice of I_o causes the subthreshold current to match the simulated value at $V_{GS}=V_{T0}$ for our choice of η and n . We selected n such that the difference between the model and the simulation was very small at $V_{GS}=0$. This allows our model for varying V_{DS} to match more closely in magnitude. This approach may not be ideal, however. By matching the magnitude of the current at $V_{GS}=0$, we actually do a fairly poor job of matching the slope of the curve vs V_{GS} . If matching the magnitude of the curve vs V_{DS} is not so important, we could do a better job of matching the slope vs V_{GS} . Also, the choice of η changes the slope of the curve as V_{DS} varies. Again, different choices of this parameter allow a better match over different regions of the curve. You see that the limitations of this model force some trade-offs in the decision

about the “best match”.



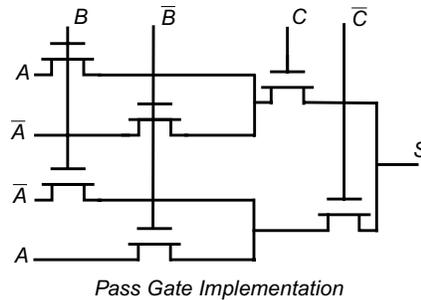
Models and Simulated Data.

Problem 6: DCVSL Gate Design

- a) Implement the function $S = ABC + \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C}$ using transmission gate logic. What function does this circuit implement.

Solution

This is the ‘Sum’ bit of a one bit carry-in adder. A pass transistor implementation is shown below. The transmission gate implementation you designed will have a PMOS in parallel with each NMOS driven by the complement of the signal that drives the NMOS.



- b) Now, design a DCVSL gate which implements the same function. Assume A , B , C , and their complements are available as inputs.

Solution

One implementation of this circuit is shown on page 50 of Handout #3.

- c) Simulate your DCVSL implementation in HSPICE with 30 fF load capacitance on each output. Assume that $W/L = 0.5\mu/0.25\mu$ for all NMOS transistors and $W/L = 2\mu/0.25\mu$ for all PMOS. Does your circuit work? If not, explain why and resize the PMOS devices to fix the problem.

Solution

The circuit will not work with this sizing because the PMOS is too large and the NMOS pull-down network will be unable to pull the outputs down to the required value for switching to occur. A more reasonable size for the PMOS is around 0.5 μm .

- d) Assuming $W/L = 0.5\mu/0.25\mu$ for all *nmos* transistors and $W/L = WP/0.25\mu$ for the *pmos* transistors (where WP is the value you chose in part c), produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1. Extract and simulate your circuit to verify functionality.

Solution

One possible layout is shown below:

