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6.334 Power Electronics
Spring 2007

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.334 Power Electronics

Issued: April 6, 2007

Problem Set 7

Due: April 13, 2007

Reading: KSV Chapter 25, Chapter 9.1 – 9.5, 9.7.1

Problem 7.1

Figure 1 shows the structure, waveforms, and operating sequence of a power converter topology known as a resonant pole inverter. The top switch is turned on until inductor current i_L rises to a positive value i_{p+} . The top switch is then turned off (under ZVS conditions) and the resonant capacitors ring with the resonant inductor until the bottom diode conducts, at which point the bottom switch can be turned on (under ZVS conditions). The other half of the cycle is essentially the reverse of the first half.

Derive the minimum current i_{p+} that will enable zero voltage turn-on of the bottom device. Express this minimum current as a function of C_r , L_r , V_{dc} , and V_{cf} . You may assume that V_{cf} does not change during a cycle.

Calculate the turn-off loss of the top switch, assuming that at turn off the current in the switch falls linearly to zero in a time t_f . As this converter is designed to operate with “zero-voltage” switching, you may assume the switch current reaches zero *before* the switch voltage rises to the bus voltage V_{dc} .

Problem 7.2 KSV Problem 25.4

Problem 7.3 KSV Problem 25.5

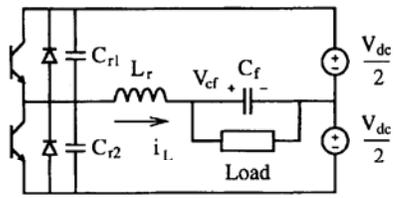
Problem 7.4

Attached is a portion of the data sheet for an International Rectifier power MOSFET IRF620S; the full datasheet can be obtained at www.irf.com. Assume a maximum allowable junction temperature of 140 °C and a maximum ambient temperature of 50 °C for this problem. (Note that the on-state resistance of the MOSFET varies with junction temperature, as illustrated in datasheet Fig. 4.)

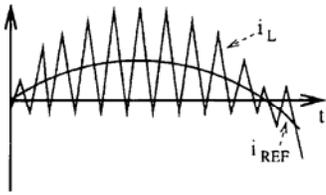
- A. Assume that the device must carry a (forward) rms current of 2.0 A, and that switching losses can be ignored. The MOSFET is attached to a heat sink using an insulating pad with a maximum thermal resistance of 1 °C/W. What is the maximum allowable thermal resistance of the heat sink?
- B. Suppose the device is instead operated in a pulsed fashion, carrying large pulses of current 1 ms in duration with 99 ms of off time between pulses. If the device is mounted to an extremely good heat sink that maintains the case temperature at 40 °C, what is the maximum allowable current pulse magnitude? You may assume that the MOSFET on-state resistance is always at its 140 °C value.

Problem 7.5 KSV Problem 9.2

Also, calculate the average power dissipated in the two circuits.

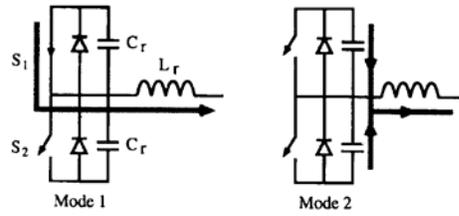


(a)



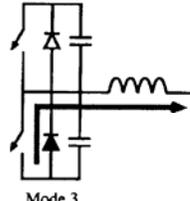
(b)

(a) The RPI and (b) its output current waveform.

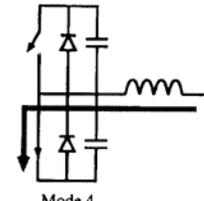


Mode 1

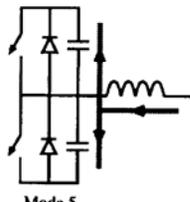
Mode 2



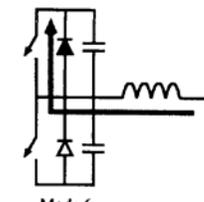
Mode 3



Mode 4



Mode 5



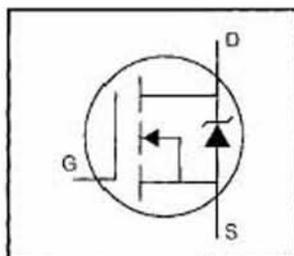
Mode 6

Fig. 1. Operational cycle of the RPI.

Figure 1 The resonant pole inverter

HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 200V$$

$$R_{DS(on)} = 0.80\Omega$$

$$I_D = 5.2A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



SMD-220

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.3	
I_{DM}	Pulsed Drain Current ①	18	
$P_D @ T_C = 25^\circ C$	Power Dissipation	50	W
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	3.0	
	Linear Derating Factor	0.40	
	Linear Derating Factor (PCB Mount)**	0.025	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	110	mJ
I_{AR}	Avalanche Current ①	5.2	A
E_{AR}	Repetitive Avalanche Energy ①	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

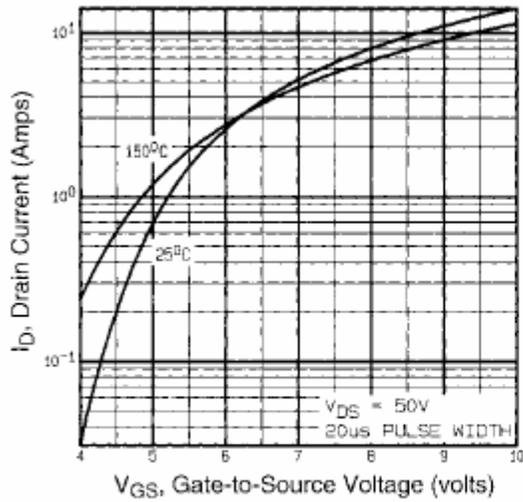


Fig 3. Typical Transfer Characteristics

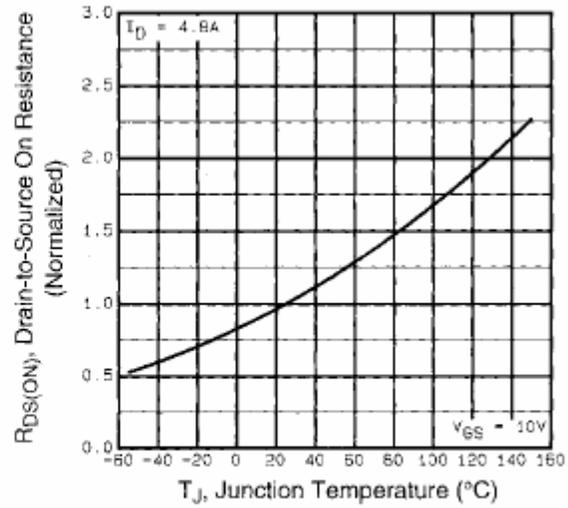


Fig 4. Normalized On-Resistance Vs. Temperature

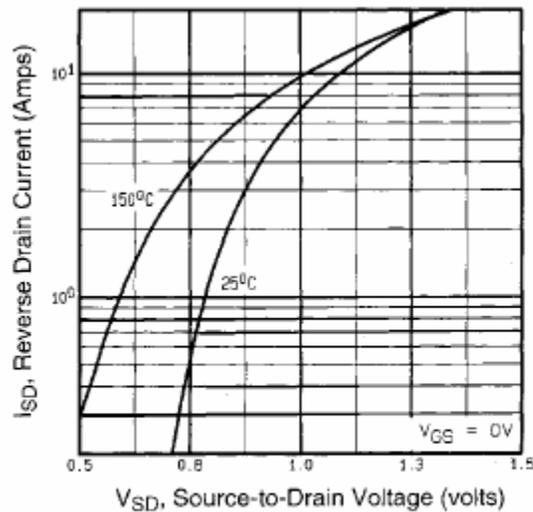


Fig 7. Typical Source-Drain Diode Forward Voltage

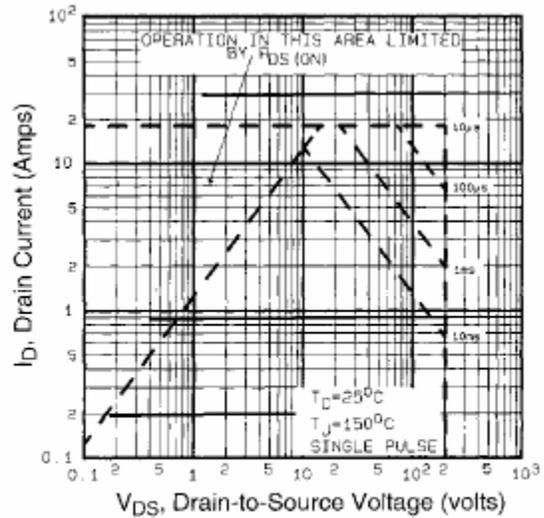


Fig 8. Maximum Safe Operating Area

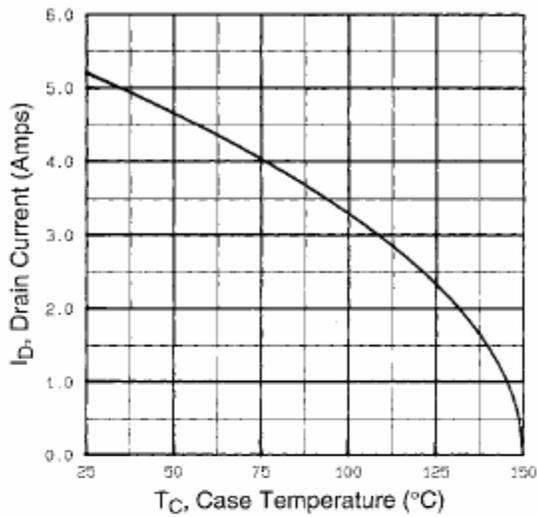


Fig 9. Maximum Drain Current Vs. Case Temperature

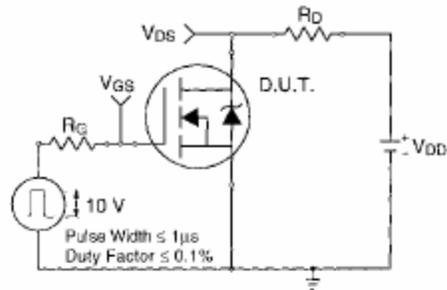


Fig 10a. Switching Time Test Circuit

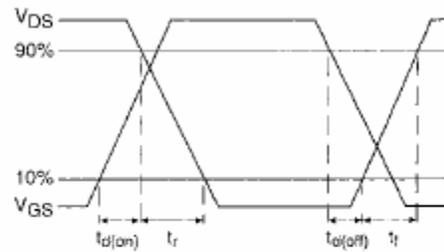


Fig 10b. Switching Time Waveforms

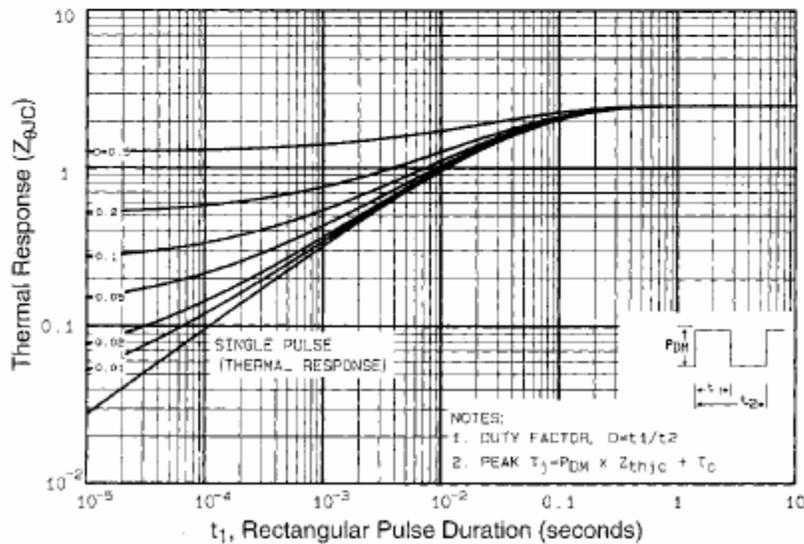


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case