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6.334 Power Electronics
Spring 2007

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Department of Electrical Engineering and Computer Science

6.334 Power Electronics
Problem Set 6

Issued: April 2, 2007
Due: April 6, 2007

Reading: KSV Chapter 24, handouts on filter design

Problem 6.1 KSV Problem 8.9

Problem 6.2

Figure 1 shows the schematic of a Full-Bridge Three-Level “Flying Capacitor” Inverter. This is a simple example of a *multilevel* inverter topology. In this topology, the voltages on the flying capacitors are controlled to be approximately half of the input voltage (by balancing the switching patterns appropriately).

- a. Propose a switching pattern for the devices in the flying capacitor inverter that takes advantage of the multilevel capabilities of the inverter and results in an (unfiltered) output voltage $v_x(t)$ having no third, fifth, or even harmonics. You may assume that the voltages on the flying capacitors are at one half the input voltage. Note that each switch is switched oppositely with its corresponding “primed” switch. Consequently, the independent switching functions are q_{A1} , q_{A2} , q_{B1} , and q_{B2} . How many times does each active device switch on and off per ac output cycle?
- b. How does the total harmonic distortion of the unfiltered waveform $v_x(t)$ compare to that of a conventional inverter using the harmonic elimination scheme of Fig. 8.6(c)?

Problem 6.3

Figure 3 shows a buck converter with an LC input filter. The 25 W buck converter operates in heavy continuous conduction mode at a switching frequency of 200 kHz, and generates a 5 V output from a 9 V input. The filter capacitor C_F is a 220 μ F Sanyo OSCON capacitor; this capacitor has an rms current rating of 3.7 A, and its impedance characteristic is shown in Fig. 3. The filter inductor L_F is 220 μ H, and may be considered ideal for purposes of this problem. The input source supplying the buck converter has negligible output impedance.

- a. Estimate the equivalent series resistance and equivalent series inductance of the filter capacitor C_F .
- b. Select numerical values for the damping components C_D , R_D such that there is less than 10 dB of peaking in the transfer function from filter input current (buck converter current i_X) to filter output current (supply current i_Y).
- c. Plot the transfer function magnitude from filter input current to filter output current, including the effect of filter capacitor parasitics. How does this compare to a filter with an “ideal” capacitor?
- d. Calculate the incremental “negative resistance” provided to the filter by the closed-loop converter operating at full power. Do you expect this to have a significant impact on filter damping?

Problem 6.4 KSV Problem 24.2

Also, plot the device voltage and current during turn-on and turn-off transitions for this case, along with the switching locus in the V-I plane. *Hint: You may assume that the switch voltage still transitions linearly during the switching process.*

Problem 6.5 KSV Problem 24.3

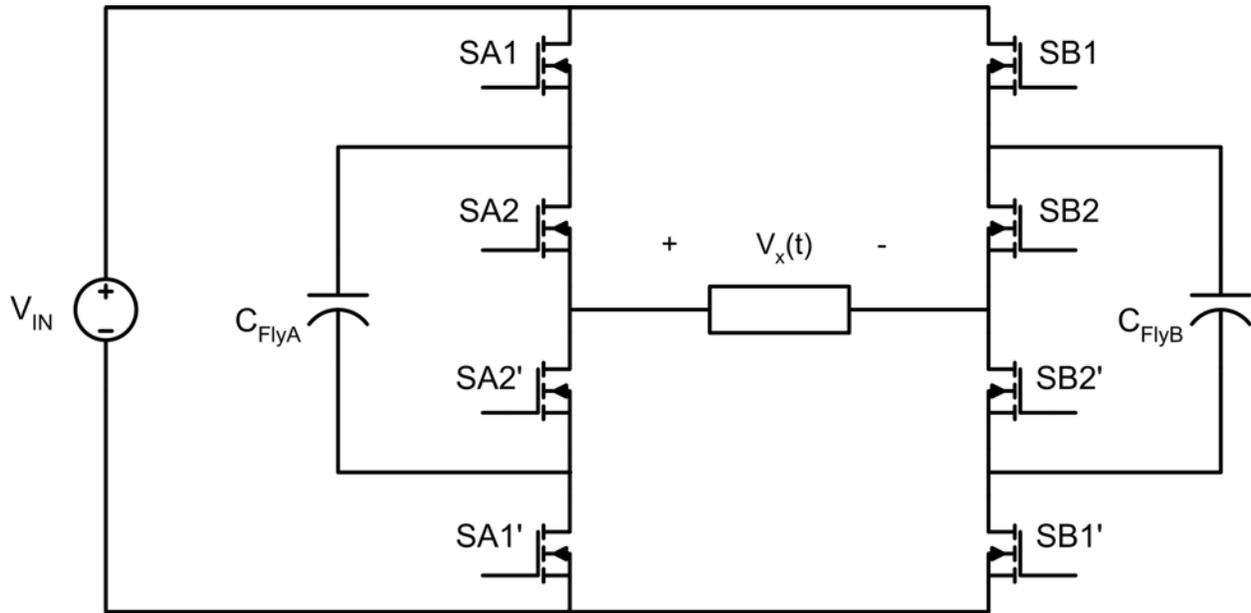


Figure 1 A Three-Level “Flying Capacitor” (or “Capacitor Clamped”) Inverter.

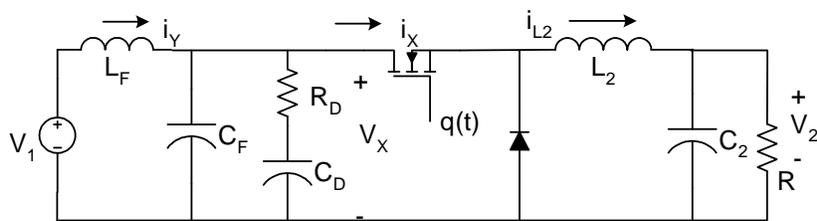


Figure 2 A buck converter with LC input filter.

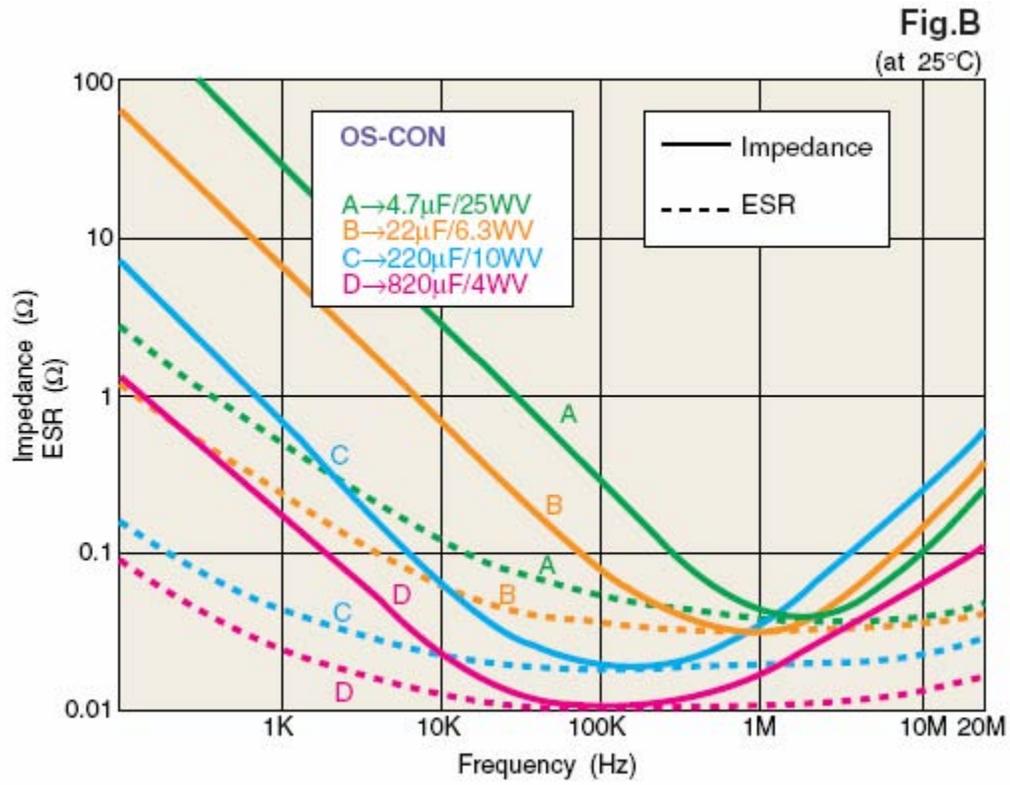


Figure 3 Impedance characteristics of Sanyo OSCON capacitors