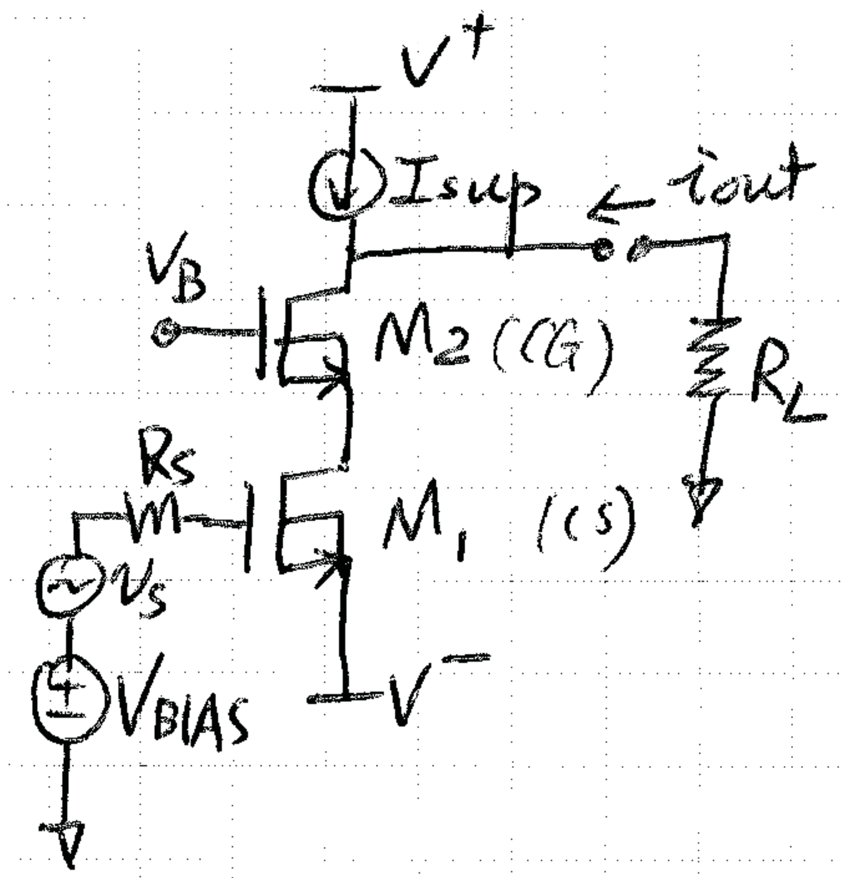
Recitation 25: CMOS Cascade Amplifier

Last week, we talked about a particular example of multi-stage amplifier: CS-CB cascode amplifier. We used BJT/CMOS in the circuit (BICMOS)
Today we will look at the CMOS cascode amplifier with some specific requirement on R_{out}, and see how to generate I_{sup} and V_{B}



This is a CS-CG CMOS cascode amplifier. It has

- R_{in} ∞
- R_{out} very high (compare to CS only)
- Very good frequency response (close to CG, better than CS)

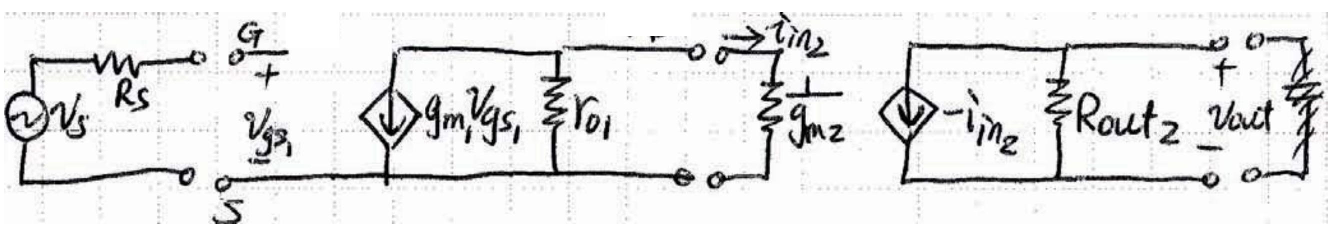
Example: Device Data

$$V_{T_p} = -1\,\text{V} \quad \mu_p C_{ox} = 25\,\mu\text{A/V}^2 \quad \lambda_p = 0.02\,\text{V}^{-1}$$
$$V_{T_n} = 1\,\text{V} \quad \mu_n C_{ox} = 50\,\mu\text{A/V}^2, \quad \lambda_n = 0.05\,\text{V}^{-1},\ \text{L} = 2\,\mu\text{m}$$

Goal:

- design transconductance amplifier with $G_m = 1\,\text{mS}$, $\text{R}_{out} \geq 10\,\text{M}\Omega$, $\text{R}_{in} = \infty$.
- With $5\,\text{V}$ power supply, $2\,\mu\text{m}$ CMOS process.
- output drives other CMOS (capacitive load).
- Use $I_{sup} = 100\,\mu\text{A}$.

Small signal model of the circuit



$$R_{in} = \infty$$
$$R_{out_2} = \gamma_{oc}||(\gamma_{o2} + \gamma_{o2}\cdot g_m R_s) = \gamma_{oc}||(\gamma_{o2}\cdot g_{m2}\cdot\gamma_{o1})) \quad R_s = \gamma_{o1}$$
$$\text{Overall}\, G_m = \frac{v_{out}}{v_s} = \frac{-i_{in2}}{v_s} = \frac{g_{m1}v_{gs1}\left(\frac{\gamma_{o1}}{\gamma_{o1}+\frac{1}{g_{m2}}}\right)}{v_s} = g_{m1}$$
$$\because G_m = g_{m1} = 1\,\text{mS} \implies \text{g}_{m1} = \sqrt{2\left(\frac{\text{W}}{\text{L}}\right)_1 \mu_n \text{C}_{ox}\text{I}_D} = 1\,\text{mS}$$
$$\text{Solve for } w_1,\ w_1 = \frac{g_{m1}^2\cdot L_1}{2I_D\mu_n C_{ox}} = \frac{(1\,\text{mS})^2\cdot(2\,\mu\text{m})}{2\times 100\,\mu\text{A}\cdot 50\,\mu\text{A/V}^2} = 200\,\mu\text{m}$$

This is design on M1.

M2: output resistance requirement determines size of M2

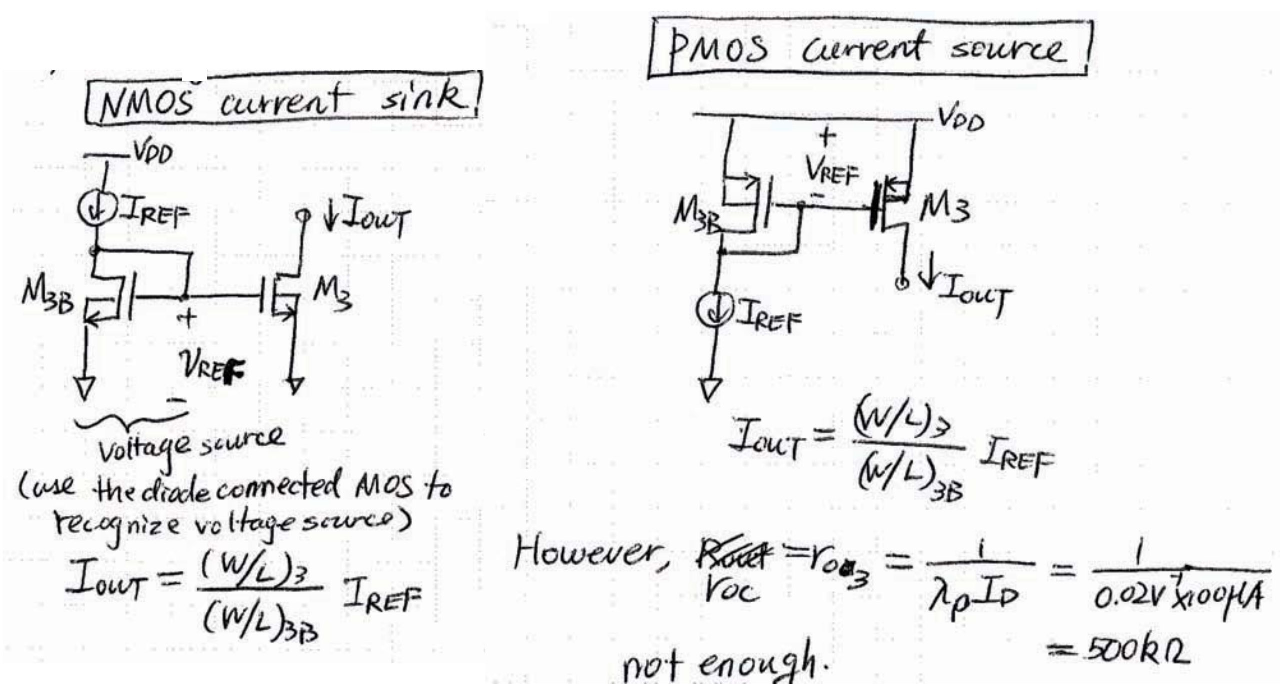
$$R_{\rm out} \simeq \gamma_{\rm oc} || (g_{\rm m2} \cdot \gamma_{\rm o2} \cdot \gamma_{\rm o1}) \geq 10\,{\rm M}\Omega$$

Assume both $\gamma_{\rm oc}, g_{\rm m2} \cdot \gamma_{\rm o2} \cdot \gamma_{\rm o1}$ are on the same order,

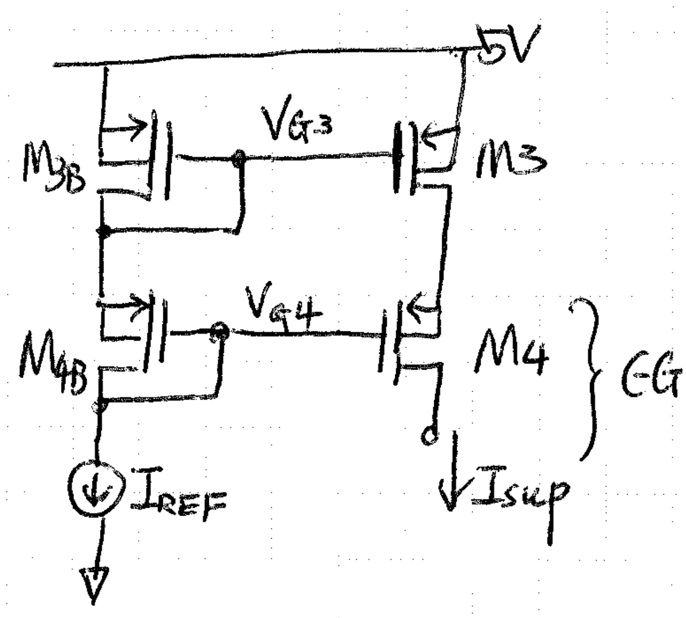
$$\begin{aligned}
\gamma_{\rm oc} &\simeq g_{\rm m2} \cdot \gamma_{\rm o2} \cdot \gamma_{\rm o1} \implies g_{\rm m2} \cdot \gamma_{\rm o1} \cdot \gamma_{\rm o2} \geq 20\,{\rm M}\Omega \\
\lambda_{\rm n} &= 0.05\,{\rm V}^{-1} \implies \gamma_{\rm o1} = \gamma_{\rm o2} = \frac{1}{\lambda_{\rm n} {\rm I_D}} = \frac{1}{(0.05\,{\rm V}^{-1})(100\,\mu{\rm A})} = 200\,{\rm k}\Omega \\
g_{\rm m2} \cdot (200\,{\rm k}\Omega)(200\,{\rm k}\Omega) &\geq 20\,{\rm M}\Omega \implies {\rm g_{m2}} \geq 5 \times 10^{-4}\,{\rm S} = 0.5\,{\rm mS} \\
g_{\rm m2} &= \sqrt{2 I_{\rm D} \left(\frac{w}{L}\right)_2 \mu_{\rm n} C_{\rm ox}} \implies \left(\frac{w}{L}\right)_2 = 25, \;\; w_2 = 50\,\mu{\rm m}
\end{aligned}$$

Current Source Design

Now how to design current source $I_{\rm sup}$ so that $\gamma_{\rm oc} \geq 20\,{\rm M}\Omega$? Yesterday we talked about simple MOS current source



$\implies$ need to cascode circuit for current source. Add a current buffer (CG) for high $R_{\rm out}$
Source resistance of current supply



$$
\begin{aligned}
R_{\text{current source}} &= R_{\text{out}} \text{ of CG} \\
&= (g_{m4} \cdot \gamma_{o4}) \cdot \underbrace{\gamma_{o3}}_{R_s} \\
&= g_{m4} \cdot 500\,\text{k}\Omega \cdot 500\,\text{k}\Omega \geq 20\,\text{M}\Omega
\end{aligned}
$$

Need g_{m4}, which is determined by size M4
Size of M3 and M4 is related to V_{G3} and V_{G4} to bias these gates, M3 and M4 need to be in saturation regime:

$$V_{SD} > V_{SG} + V_{T_p} \quad \text{Choose} V_{SG} = 1.5\,\text{V} \implies \text{minimum} \text{V}_{SD} = (1.5 - 1), \text{V} = 0.5\,\text{V}$$

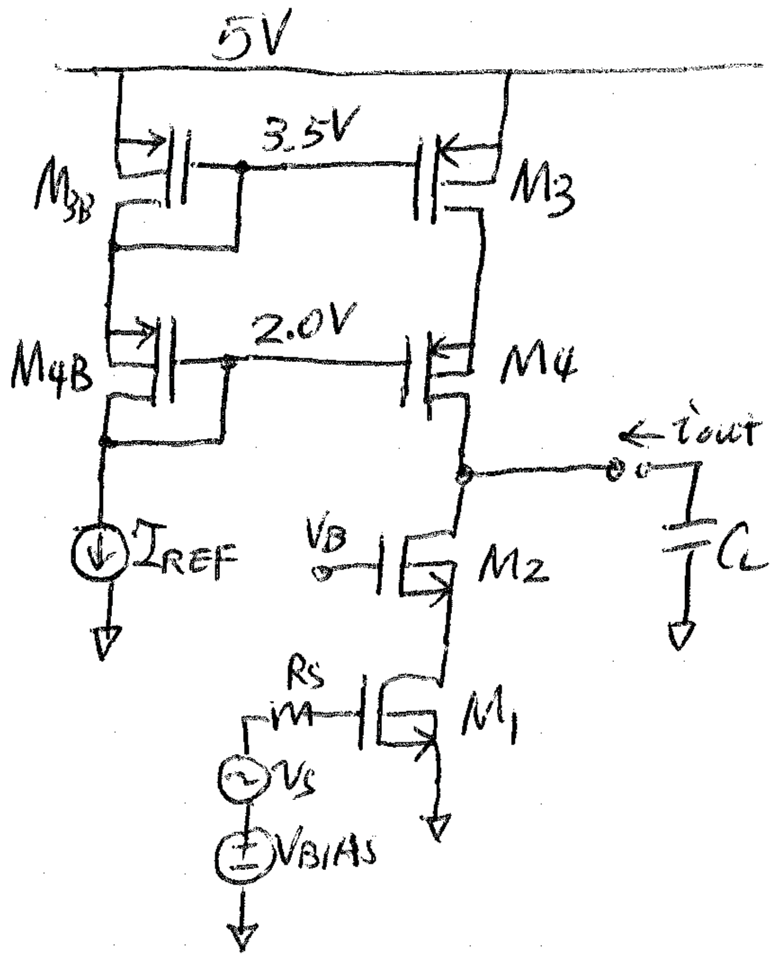
(If we choose smaller V_{SG}, we will need larger device $\frac{w}{L}$ to carry $100\,\mu\text{A}$)

$$
\begin{aligned}
\text{with } V_{SG} &= 1.5\,\text{V} \implies \text{V}_{G_3} = 3.5\,\text{V and V}_{G4} = 2\,\text{V} \\
\text{Since } |I_{DP}| &\simeq \frac{w}{2L}\mu_p C_{ox}(V_{SG} + V_{T_p})^2 = 100\,\mu\text{A} \\
\left(\frac{}{L}\right)_{3,4} &= \frac{2|I_{Dp}|}{\mu_p C_{ox}(V_{SG} + V_{T_p})^2} = 32 = \frac{64}{2} \\
g_{m4} &= \frac{w}{L}\mu_p C_{ox}(V_{SG} + V_{T_p}) = 0.4\,\text{mS}
\end{aligned}
$$

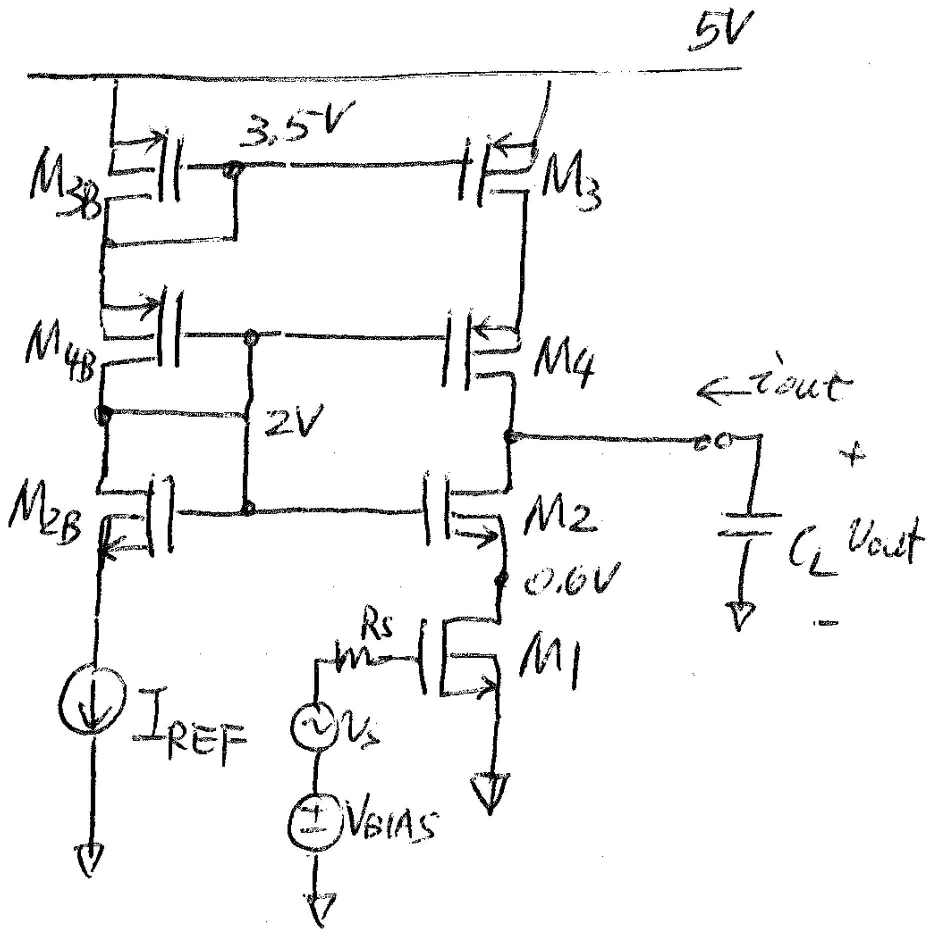
(Size of M3B & M4B should be the same as for M4 and M3, helps in matching current flow). Then

$$
\begin{aligned}
R_{\text{currentsource}} &= g_{m4} \cdot \gamma_{o4} \cdot \gamma_{o3} = (0.4\,\text{mS})(500\,\text{k}\Omega)(500\,\text{k}\Omega) \\
&= 100\,\text{M}\Omega > 20\,\text{M}\Omega
\end{aligned}
$$

What does the design look like so far?



$\Longrightarrow$ Need voltage source for V_B. Use diode connected NMOS (M2B) between I_{REF} and PMOS



Make M2B same size as M2, $\left(\frac{w}{L}\right)_{2B} = 50/2$ and:

$$V_{GS_2} = V_{GS_{2B}} = V_{T_n} + \sqrt{\frac{2I_{REF}}{\left(\frac{w}{L}\right)_2 \mu_n C_{ox}}} = 1.4\,\text{V}$$

Output Voltage Swing

$$\begin{aligned}
\text{upswing :} &\quad \text{M4 must stay in saturation regime} \\
V_{\mathrm{SD_4}} &\geq V_{\mathrm{SG_4}} + V_{\mathrm{T_p}} \implies V_{\mathrm{SD_4}} \geq 1.5\,\mathrm{V} - 1\,\mathrm{V} = 0.5\,\mathrm{V} \\
\text{Since}\, V_{\mathrm{S_4}} &= 3.5\,\mathrm{V} \implies \mathrm{V_{D_4}} \leq 3\,\mathrm{V} \\
\text{down swing :} &\quad \text{M2 must stay in saturation regime} \\
V_{\mathrm{DS_2}} &\geq V_{\mathrm{GS_2}} - V_{\mathrm{T_n}}, \quad V_{\mathrm{DS_2}} \geq 1.4\,\mathrm{V} - 1.0\,\mathrm{V} = 0.4\,\mathrm{V} \\
\text{Since}\, V_{\mathrm{S_2}} &= 0.6\,\mathrm{V}, \quad \mathrm{V_{D_2}} \geq 1\,\mathrm{V} \\
\implies &\quad \text{Swing is}\, 1.0\,\mathrm{V} \leq \mathrm{V_{out}} \leq 3.0\,\mathrm{V}
\end{aligned}$$