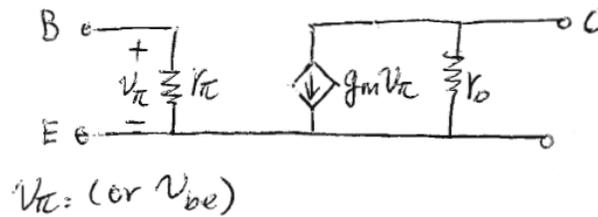


## Recitation 19: Common Emitter Amplifier

### Review: Small signal model of BJT

#### Low Frequency

Voltage/Current Controlled Current Source



$$g_m = \frac{I_c}{V_{th}} = \frac{I_c}{kT/q} \quad \text{transconductance}$$

$$\gamma_{\pi} = \frac{1}{g_{\pi}} = \frac{\beta_F}{g_m}$$

$$\gamma_o = \frac{1}{g_o} = \frac{1}{\frac{\delta i_c}{\delta V_{CE}}} \approx \frac{V_A}{I_C} \quad \text{base-width modulation}$$

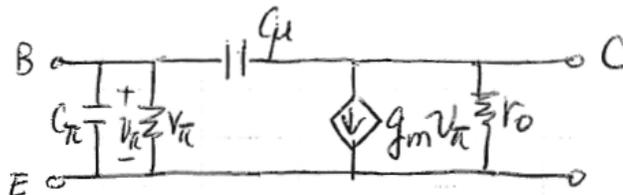
#### High Frequency

Adding capacitances: between base-emitter, a forward-biased p-n junction

$$C_{\pi} = \text{depletion cap.} + \text{diffusion cap.}$$

Between base-collector, reverse biased p-n junction

$$C_{\mu} = \text{depletion cap.}$$

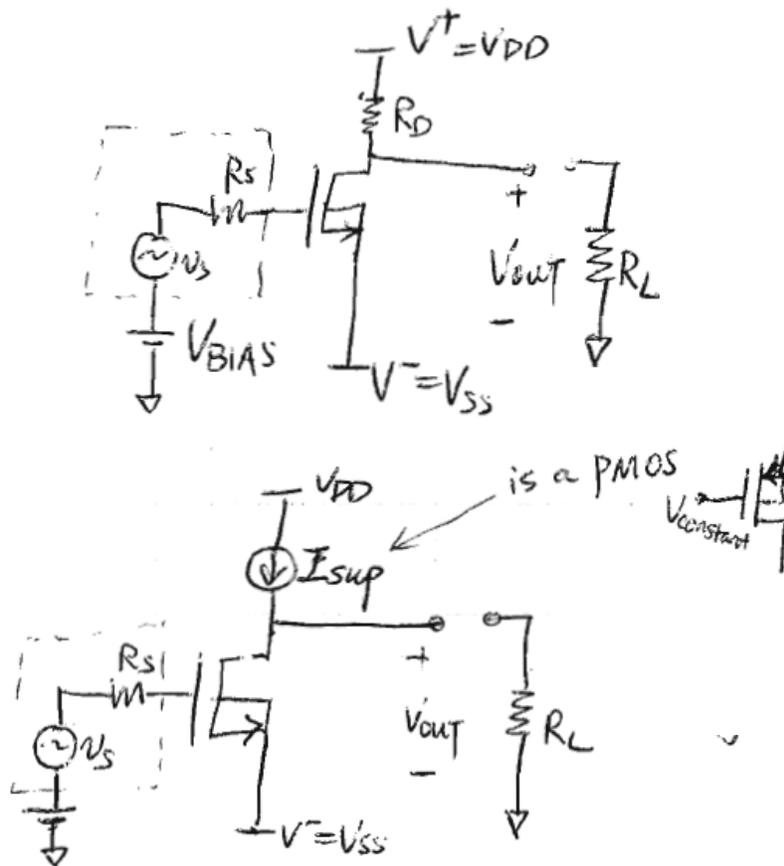


## Transistor Amplifiers

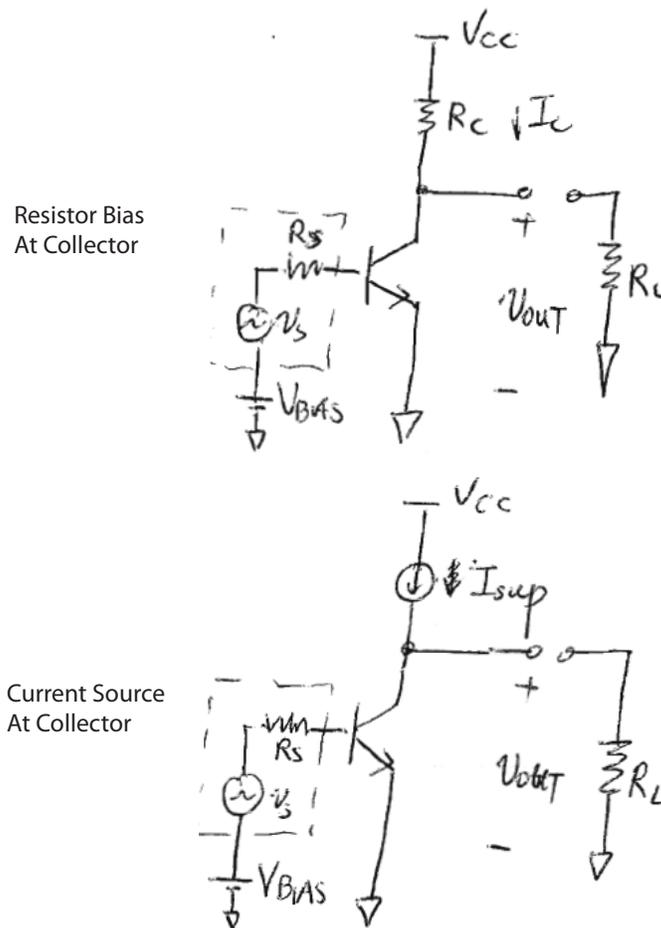
Yesterday we started our discussion on transistor amplifiers. For amplifiers, we have:

Type	Input	Output
Voltage Amplifier	V	V
Current Amplifier	I	I
Transconductance Amplifier	V	I
Transresistance Amplifier	I	V

Voltage and transconductance amplifiers are most common. Yesterday, we discussed the common-source amplifier shown below:



Today, we will discuss common-emitter amplifier (for the BJT version)



For amplifier circuits, what we are interested in are:

- What is the operating point? (Bias point)
- Signal Swing?
- Small signal gain; input resistance; output resistance
- Frequency Response

Among these, first two are *large signal* analysis, while the last two are related to *small signal* circuits.

### DC Bias Point

For large signal analysis,  $V_s$  &  $R_s$  will be gone. Also make  $R_L \infty$ . See figure 4,

$$V_{out} = V_{cc} - I_c \cdot R_c$$

If we choose  $V_{out} = \frac{V_{cc}}{2} = 2.5 \text{ V}$  ( $V_{cc} = 5 \text{ V}$ ),  $R_c = 10 \text{ k}\Omega$

$$I_c = \frac{V_{cc} - V_{out}}{R_c} = \frac{5 \text{ V} - 2.5 \text{ V}}{10 \text{ k}\Omega} = 250 \mu\text{A}$$

$$I_c = I_s e^{qV_{BIAS}/kT} \implies V_{BIAS} = \frac{kT}{q} \ln \frac{I_c}{I_s} = 0.682 \text{ V}$$

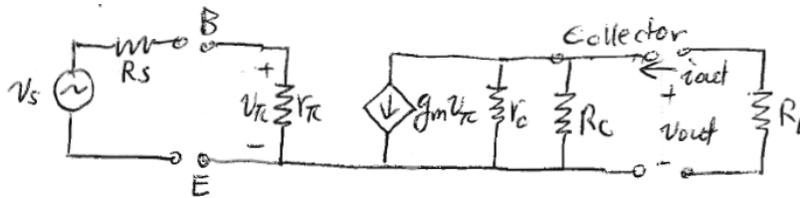
### Signal Swing

- Upswing limited by BJT going into cutoff: Total signal  $V_{out,max} = V_{cc}$
- Down swing limited by BJT going out of FAR into saturation  $V_{out,min} = V_{CE,SAT}$

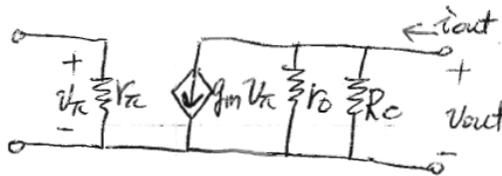
### Small Signal Analysis of CE Amplifier

First obtain the small signal circuit of the circuit in Figure 4

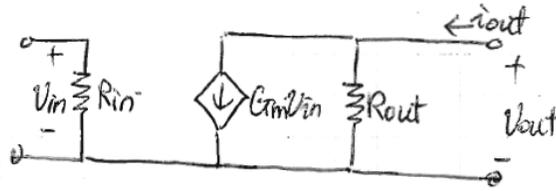
- Short DC voltage bias
- Open DC circuit bias



Intrinsic will be (without  $R_s$  and  $R_L$ )



This is a transconductance amplifier, it turns out its small signal circuit is very similar to the topography of our “two port model”



In comparison, we see

$$R_{in} = r_{\pi}$$

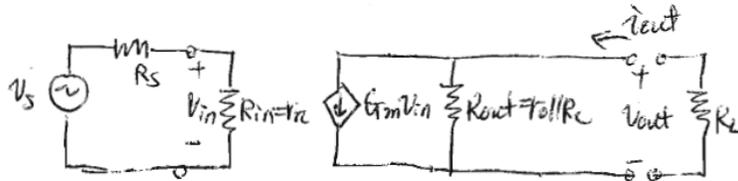
$$G_m = g_m = \frac{I_c}{kT/q}$$

$$R_{out} = r_o || R_c$$

Intrinsic or unloaded gain (short circuit output)

$$\frac{i_{out}}{V_{in}} = \frac{G_m V_{in}}{V_{in}} = G_m$$

And the loaded transconductance gain:



$$\frac{i_{out}}{V_s} = G_m V_{in} \cdot \left( \frac{R_{out}}{R_{out} + R_L} \right) \frac{1}{V_s}$$

$$= G_m \left( \frac{R_{out}}{R_{out} + R_L} \right) \cdot \frac{R_{in}}{R_{in} + R_s} V_s = g_m \left( \frac{r_o || R_c}{r_o || R_c + R_L} \right) \left( \frac{r_{\pi}}{r_{\pi} + R_s} \right)$$

### Replacing $R_c$ with a Current Source

From the discussions in the above subsection, in general:

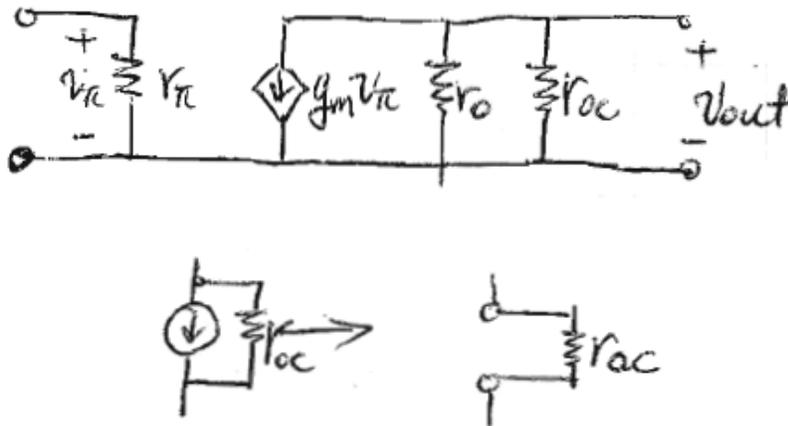
$$r_o \gg R_c \implies r_o || R_c = R_c$$

$$\text{and } \frac{i_{out}}{v_s} = g_m \left( \frac{R_c}{R_c + R_L} \right) \cdot \left( \frac{r_{\pi}}{r_{\pi} + R_s} \right)$$

If  $R_c \simeq R_L$  or  $R_c < R_L$ , transconductance gain is degraded.

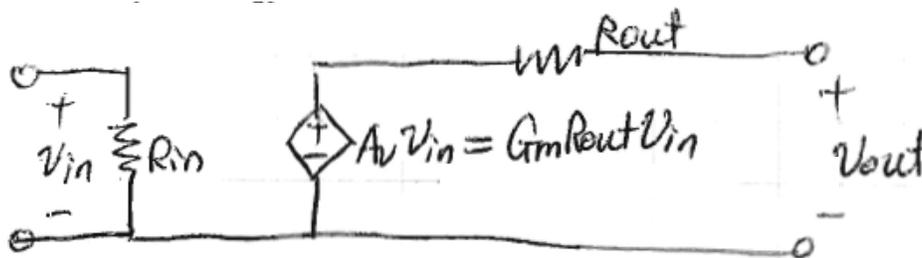
So we need a large  $R_{out}$  (output is a current)

$\implies$  use a current source at the collector  $\implies$  Figure 5 can be a p-MOSFET,  $R_c \rightarrow r_{oc}$   
 (in small signal circuit, DC current is open)



**On the CE Amp.**

We consider the CE Amp. to be a transconductance amplifier. In fact, it can also be just a voltage amplifier. In that case, the two port model becomes:

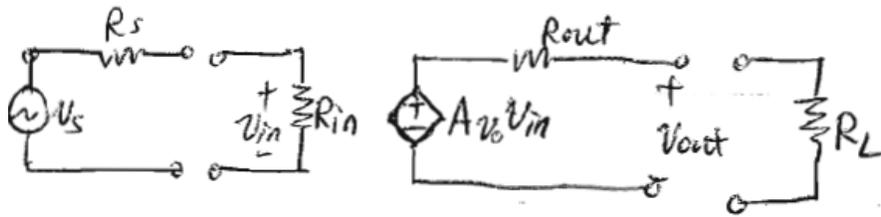


(a norton Eq circuit  
 change to a Thevenin Eq  
 circuit)

## CS vs. CE Amp

In comparison with the CS Amp we discussed yesterday:

- $V_{\text{BIAS}} = \sqrt{\frac{2I_{\text{D}}}{\frac{w}{L}\mu_{\text{n}}C_{\text{ox}}}} + V_{\text{SS}} + V_{\text{T}}$   
 (by letting  $V_{\text{OUT}} = 0$ , &  $I_{\text{R}} = I_{\text{D}} = \frac{w}{2L}\mu_{\text{n}}C_{\text{ox}}(V_{\text{BIAS}} - V_{\text{SS}} - V_{\text{T}})^2 = \frac{V_{\text{DD}}}{R_{\text{D}}}$ )
- $V_{\text{OUT,MAX}} = V_{\text{DD}}$  (MOS into cutoff)  
 $V_{\text{OUT,MIN}} = V_{\text{BIAS}} - V_{\text{T}}$  (MOSFET leave saturation)
- $R_{\text{in}} = \infty$ ,  $R_{\text{out}} = r_{\text{o}} \parallel R_{\text{D}}$



$$A_{\text{VD}} = \frac{V_{\text{out}}}{V_{\text{in}}} = -g_{\text{m}}(r_{\text{o}} \parallel R_{\text{D}})$$

$$\frac{V_{\text{out}}}{V_{\text{s}}} = -g_{\text{m}}(r_{\text{o}} \parallel R_{\text{D}} \parallel R_{\text{L}})$$

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