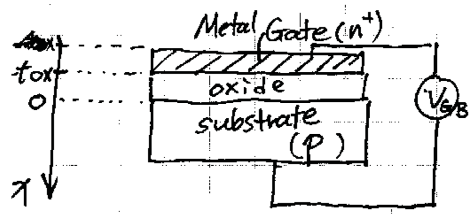
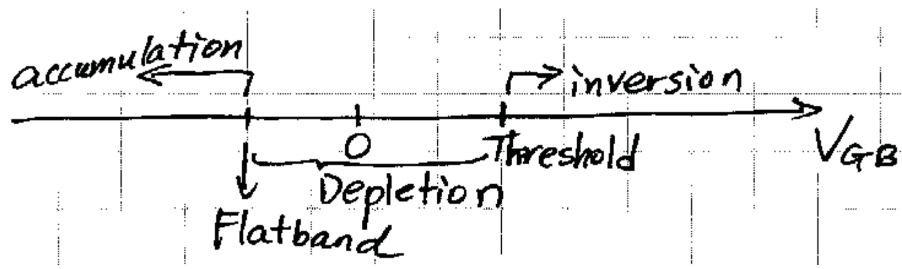
Recitation 9: MOSFET VI Characteristics

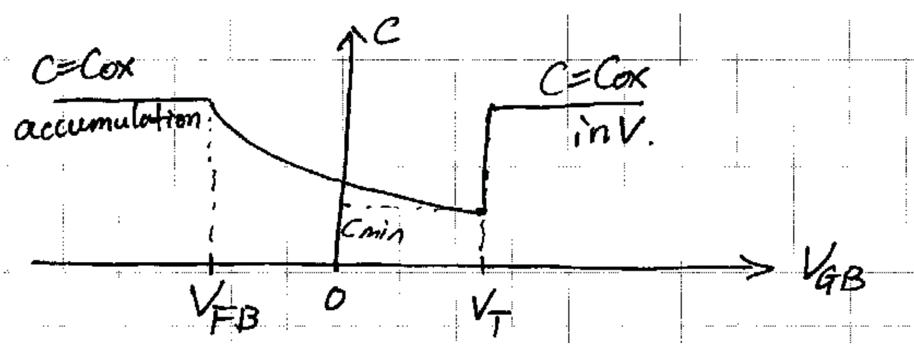
Before the class first do an exercise on MOS capacitor.

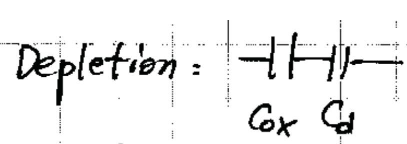


Under T.E., suppose we are under depletion, positive charges at M-O interface, negative charges (Na$^-$) at O-S interface & depletion region x_{do}.



How does the C-V measurement curve look like?





$$\frac{1}{C_{\text{tot}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{d}}}$$
$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}, \quad C_{\text{d}} = \frac{\epsilon_{\text{s}}}{x_{\text{d}}(V_{\text{GB}})}$$

Useful relations:

$$V_{\text{FB}} = -(\phi_{\text{gate}} - \phi_{\text{body}})$$
$$V_{\text{T}}(n^+/p) = V_{\text{FB}} - 2\phi_{\text{p}} + \frac{1}{C_{\text{ox}}}\sqrt{2\epsilon_{\text{s}} q N_{\text{a}}(-2\phi_{\text{p}})}$$
$$\frac{C_{\text{min}}}{C_{\text{ox}}} = \frac{1}{\sqrt{1 + \frac{2C_{\text{ox}}^2(V_{\text{T}}-V_{\text{FB}})}{q\epsilon_{\text{s}} N_{\text{a}}}}}$$

Where is C_{min}? When V_{GB} changes, C_{ox} does not change. C_{d} changes due to $x_{\text{d}}(V_{\text{GB}})$.

$$x_{\text{d}} = 0 \text{ at } V_{\text{FB}},$$
$$x_{\text{d}} = x_{\text{d,max}} \text{ at } V_{\text{T}} \implies C_{\text{min}}$$

In tutorial, you can also find what the GV curves look like for $\text{p}^+ - \text{n}$ MOS or $\text{p}^+ - \text{p}$ MOS, or $\text{n}^+ - \text{n}$ MOS.

MOSFET Device

- We only talked about 2 terminals in our MOS capacitor. Where are the other terminals? Source/Drain. In the MOS capacitor, S/D tie to bulk → ground.

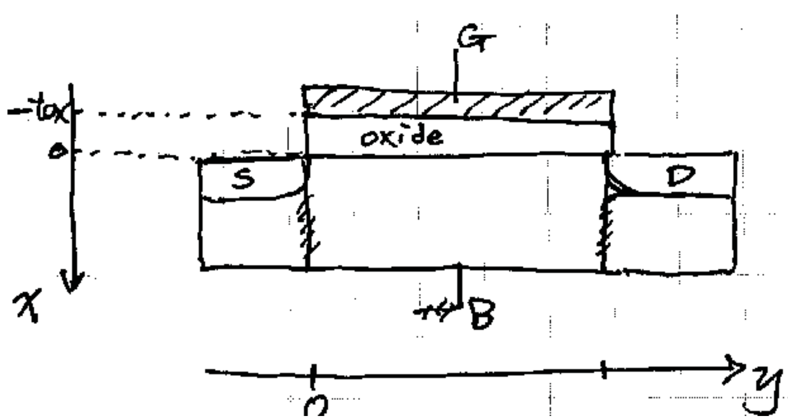


Figure 1: MOSFET: 4 terminal device

- As we mentioned, $V_{\text{GB}} \implies V_{\text{G}} - V_{\text{B}}$. In MOSFET, we usually have,

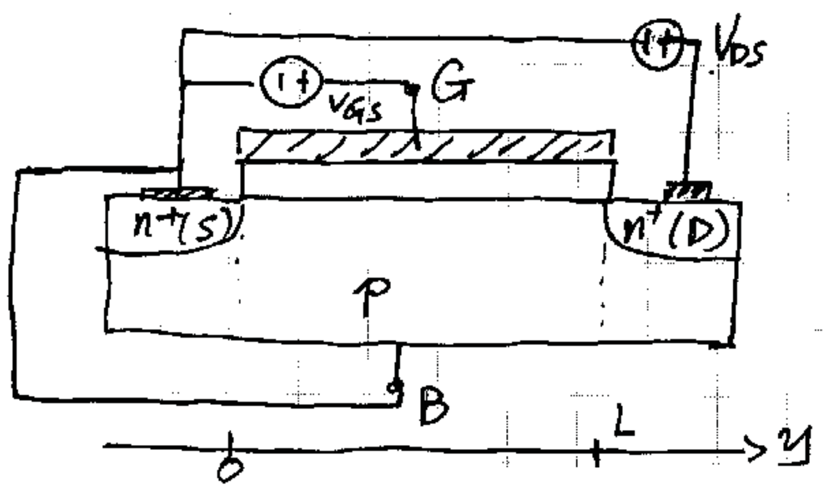
$$V_{\text{DS}} = V_{\text{D}} - V_{\text{S}}$$
$$V_{\text{GS}} = V_{\text{G}} - V_{\text{S}}$$

  You can do manipulation: $V_{\text{GD}} = V_{\text{G}} - V_{\text{D}} = V_{\text{GS}} - V_{\text{DS}}$

- If the substrate of MOSFET is p-type, what type of MOSFET device this is? n-MOS or p-MOS?

  It is n-MOS. MOSFET operates when it is in Inversion. So for n-MOS: Source/Drain are n^+. Thus we have two $\text{p} - \text{n}^+$ junctions between source-substrate (bulk), n^+ (D) and p (B). When we apply biases, we try to keep $V_{\text{BS}} \leq 0, V_{\text{BD}} \leq 0$ otherwise the $\text{p} - \text{n}^+$ junction will conduct.

- When we use n-MOS, we always try to use source as reference: $V_{\text{GS}}, V_{\text{DS}}$ etc. To start with, we let $V_{\text{BS}} = 0 \implies V_{\text{GB}} = V_{\text{GS}}$



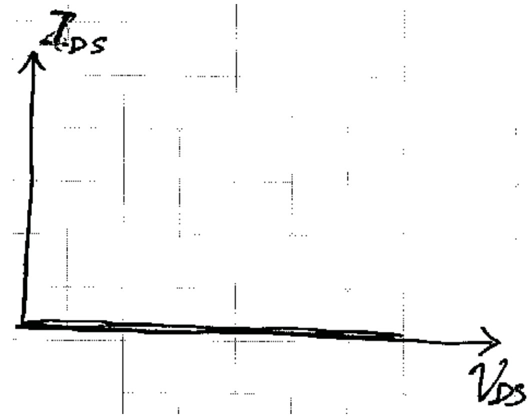
From yesterday's discussion or 6.002, what are the I-V characteristics (i.e. when applying V_{DS}, what does I_{DS} look like) of a n-MOS?

1. Remember we need to apply positive V_{GB} (i.e. V_{GS} here) in order to reach threshold. Before threshold, no conduction.

$$\implies V_{\text{GS}} < V_{\text{T}}, I_{\text{DS}} = 0 \quad \text{always (cutoff)}$$

2. $V_{\text{GS}} \geq V_{\text{T}}$, now we have inversion layer. If the $V_{\text{DS}} = 0$, what is the inversion layer charge density?

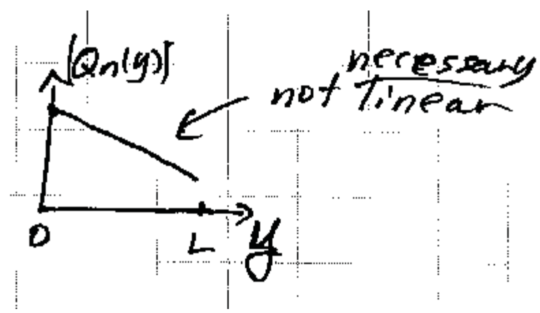
$$|Q_{\text{n}}| = C_{\text{ox}}(V_{\text{GS}} - V_{\text{T}})$$



When $V_{\mathrm{DS}} > 0$, how will this charge density change? Now from S to D, along the channel interface, potential is no longer 0.

$$\begin{aligned} V(y) &\neq 0 (0 < y < L) \quad \text{at each location y} \\ \therefore, |Q_{\mathrm{n}}(y)| &= C_{\mathrm{ox}}(V_{\mathrm{GS}} - V(\mathrm{y}) - \mathrm{V_T}) \end{aligned}$$

Decrease from source$(y = 0)V(y) = 0$ to minimum at $D(y = L, V(L) = V_{\mathrm{DS}})$.



To calculate I_{DS} remember current $\propto$ charge density, $\propto$ carrier velocity.

$$I_{\mathrm{DS}} = W \cdot |Q_{\mathrm{n}}(y)| \cdot v_y(y)\,(v_y(y) \quad \text{is velocity in the } y \text{ direction at location } y) \tag{1}$$

How to calculate $v_y(y)$? $v = \mu \cdot E$. So need to know $E_y(y)$. How to know $E_y(y)$?

$$E_y(y) = \frac{dV(y)}{dy} \ \text{(we have } V(x,y) \text{ at each location: } \tfrac{dV}{dx} \text{ will give } E_x)$$

Therefore to plug everything in the equation (1)

$$I_{\mathrm{DS}} = w \cdot C_{\mathrm{ox}}(V_{\mathrm{GS}} - V(y) - V_{\mathrm{T}}) \cdot \mu_{\mathrm{n}} \cdot \frac{dV(y)}{dy}$$

Integrating,

$$\int_0^y I_{DS}\,dy = \int_0^{v(y)} w\mu_n C_{ox}(V_{GS} - V_T - V(y'))\,dV'(y') \quad (2)$$

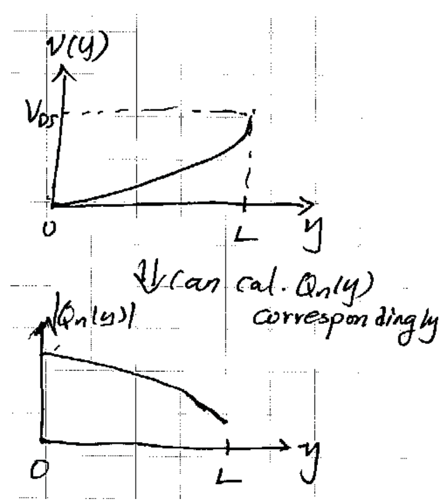
$$\frac{I_{DS}\cdot y}{w\mu_n C_{ox}} = (V_{GS} - V_T)\cdot V(y) - \frac{1}{2}V^2(y) \quad (3)$$

So we can solve the potential along each location y.

$$V(y) = (V_{GS} - V_T) - \sqrt{(V_{GS} - V_T)^2 - \frac{2I_{DS\cdot y}}{w\mu_n C_{ox}}}$$

Since I_{DS} should be the same everywhere, when $y = L, V(y) = V_{DS}$, plug in (3)

$$I_{DS} = \frac{w}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})\cdot V_{DS}$$

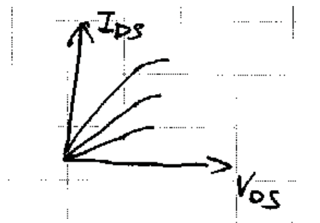


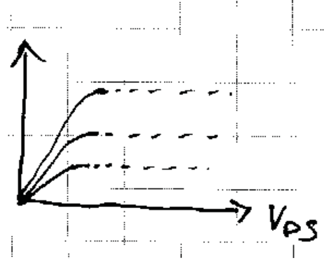
When V_{DS} is small,

$$I_{DS} \simeq \underbrace{\frac{w}{L}\mu_n C_{ox}(V_{GS} - V_T)}_{\text{Gate voltage controlled resistor}} \cdot V_{DS} \rightarrow \text{linear}$$

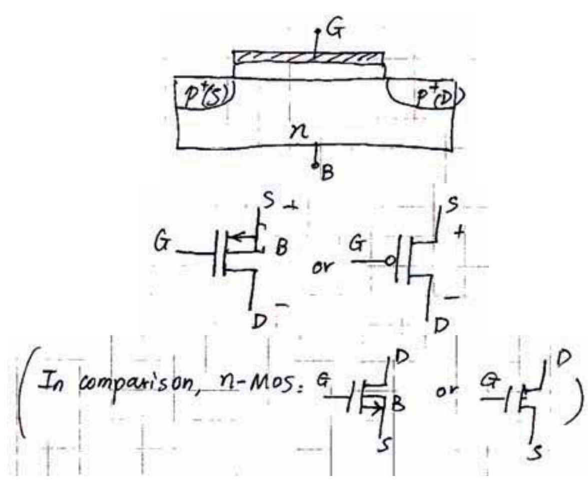
Then as V_{DS} increases, I_{DS} bend over. When $V_{DS} = V_{GS} - V_T$: I_{DS} saturates

$$I_{DSAT} = \frac{w}{L}\mu_n C_{ox}\cdot \underbrace{\frac{1}{2}(V_{GS} - V_T)^2}_{\text{(only depend on } V_{GS})}$$





PMOSFET Case



Will need $V_{\mathrm{BS}} \geq 0, V_{\mathrm{BD}} \geq 0$ always. (typically $V_{\mathrm{BS}} = 0$). Now in order to have inversion:

$$V_{\mathrm{GB}} = V_{\mathrm{GS}} < 0$$

In p-MOS, we use

$$\begin{aligned} V_{\mathrm{SG}} &= V_{\mathrm{S}} - V_{\mathrm{G}} > 0 \\ V_{\mathrm{SD}} &= V_{\mathrm{S}} - V_{\mathrm{D}} > 0 \end{aligned}$$

When working with p-MOS, simply transform

$$
\begin{aligned}
n &\longrightarrow p \\
V_{\mathrm{T_n}} &\longrightarrow -V_{\mathrm{T_p}} \\
I_{\mathrm{D_n}} &\longrightarrow -I_{\mathrm{D_p}} \\
V_{\mathrm{GS}} &\longrightarrow V_{\mathrm{SG}} \\
V_{\mathrm{DS}} &\longrightarrow V_{\mathrm{SD}} \\
\text{Triode/linear: } -I_{\mathrm{D_p}} &= \frac{w}{L}\mu_{\mathrm{p}}C_{\mathrm{ox}}\left[V_{\mathrm{SG}} + V_{\mathrm{T_p}} - \frac{V_{\mathrm{SD}}}{2}\right]V_{\mathrm{SD}} \quad V_{\mathrm{SD}} \leq V_{\mathrm{SG}} + V_{\mathrm{T_p}} \\
\text{Saturation: } -I_{\mathrm{D_p}} &= \frac{w}{2L}\mu_{\mathrm{p}}C_{\mathrm{ox}}(V_{\mathrm{SG}} + V_{\mathrm{T_p}})^2 \quad V_{\mathrm{SD}} \geq V_{\mathrm{SG}} + V_{\mathrm{T_p}}
\end{aligned}
$$

6.012 Microelectronic Devices and Circuits
Spring 2009