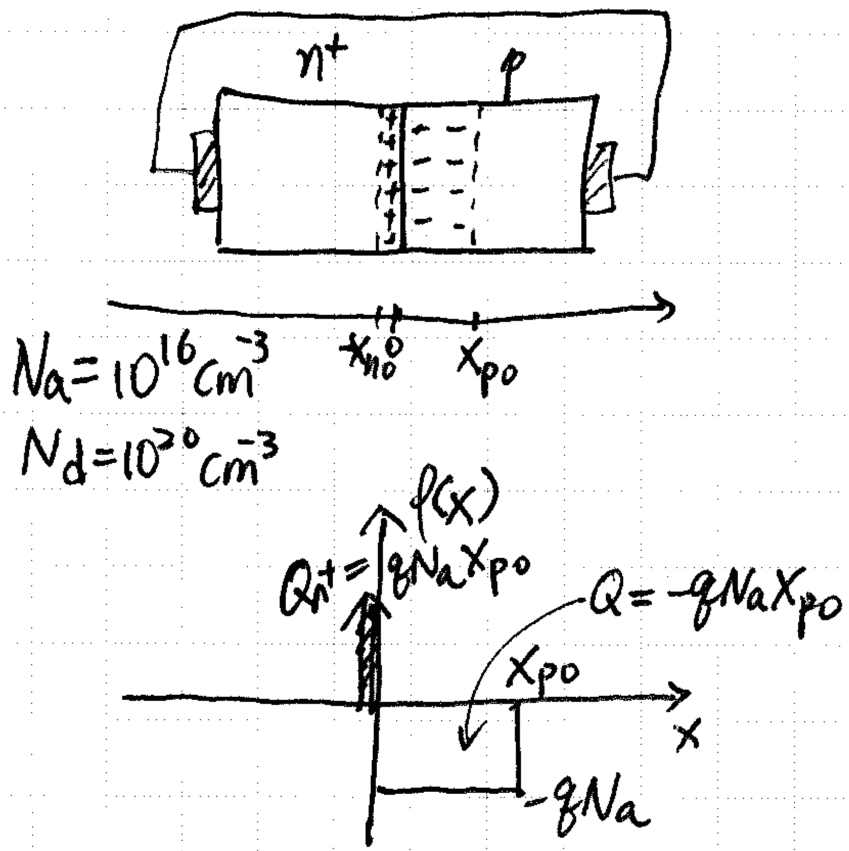
Recitation 7: From n$^+$p diode to MOS structure

Consider a p-n diode with very asymmetric doping:



$$x_{no} = \sqrt{\frac{2\epsilon_s \phi_B N_a}{q(N_a + N_d)N_d}}$$

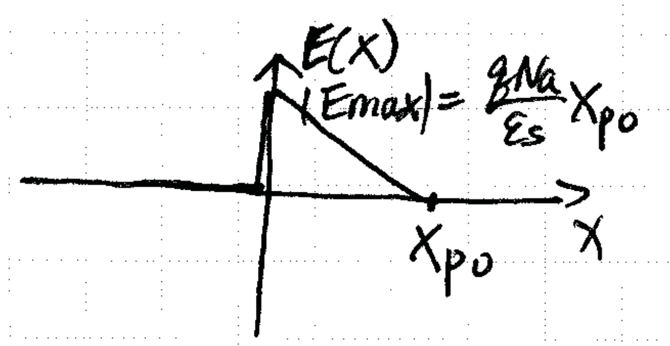
$$x_{po} = \sqrt{\frac{2\epsilon_s \phi_B N_d}{q(N_a + N_d)N_a}}$$

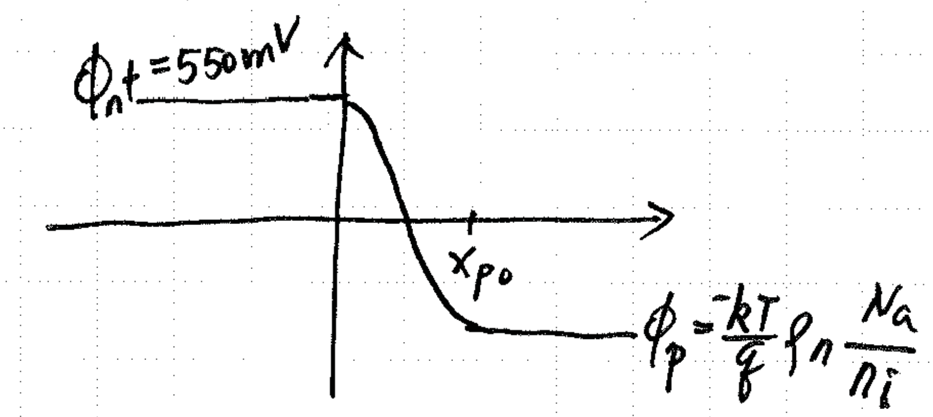
$$x_{no} \ll x_{po}$$

The SCR is entirely on the lightly doped side.

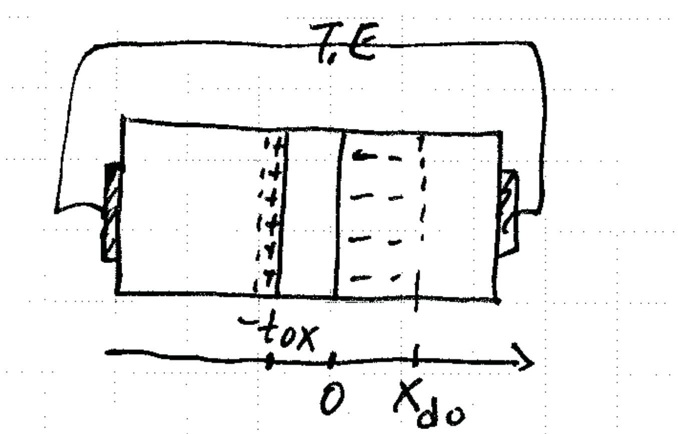
$$x_{do} \simeq x_{po} = \sqrt{\frac{2\epsilon_s \phi_B}{qN_a}}$$

Q is the charge per unit area (charge/cm^2) and $\rho(x)$ is the space charge density (charge/cm^3).





Now if we insert an insulator layer (oxide) in between n$^+$ and p, we obtain our MOS structure.

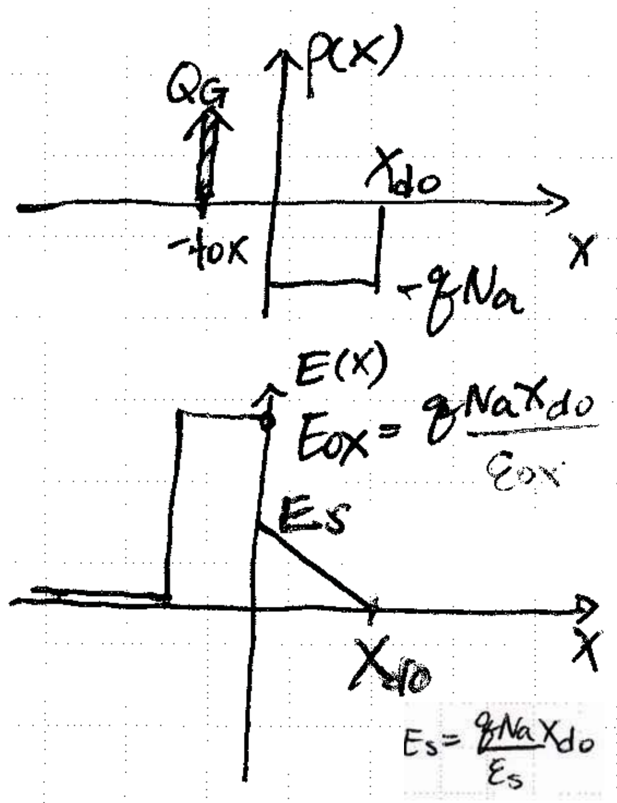


Same doping level: $N_\mathrm{d} = 10^{20}\,\mathrm{cm}^{-3}$, $\mathrm{N_a} = 10^{16}\,\mathrm{cm}^{-3}$

How does the depletion region x_do compare with x_po above?

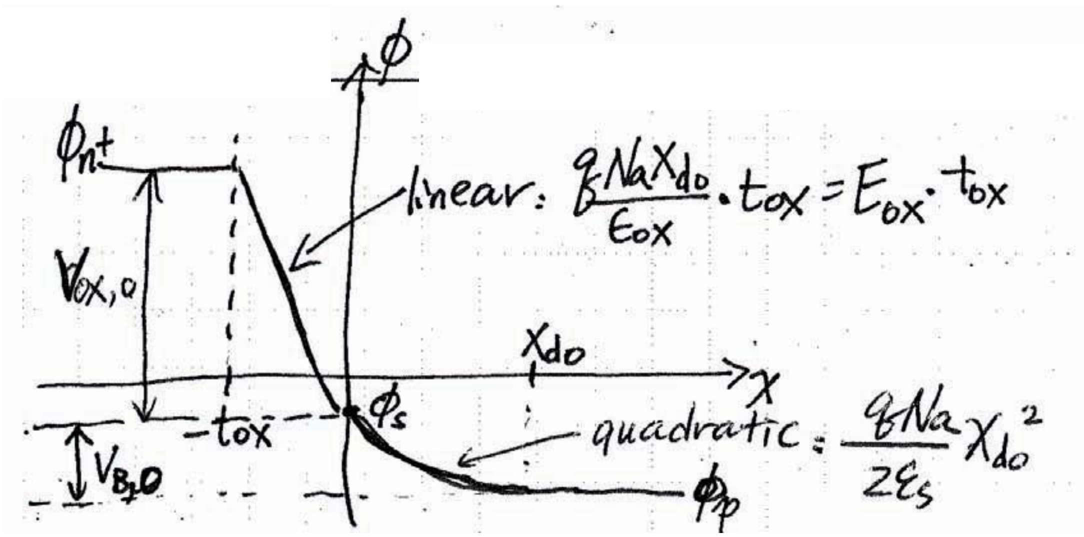
We can take some intuitive guess first. Then let us look at the problem quantitatively.

$$Q_\mathrm{G} = qN_\mathrm{a}x_\mathrm{do} \quad \mathrm{Coulomb/cm^2}$$



Electric field is the integration of charge density/ϵ_s or ϵ_ox: At the boundary,

$$\begin{aligned}
\epsilon_\mathrm{ox}E(0^-) &= \epsilon_\mathrm{s}E(0^+) \\
E(0^-) &\rightarrow E_\mathrm{ox}, E(0^+) \rightarrow E_\mathrm{s} \\
E_\mathrm{ox} &= \frac{\epsilon_\mathrm{s}}{\epsilon_\mathrm{ox}}E_\mathrm{s} \simeq 3E_\mathrm{s}
\end{aligned}$$



$V_{\text{B,O}}$ is potential drop across semiconductor *body*, while $V_{\text{ox,O}}$ is potential drop across oxide. (Note that unit wise: potential, voltage and bias are the same).
But ϕ_{B} is fixed (same as n$^+$p junction).

$$\begin{aligned}\phi_{\text{B}} = \phi_{\text{n}^+} - \phi_{\text{p}} &= V_{\text{ox,o}} + V_{\text{B,O}} \\ &= E_{\text{ox}} \cdot t_{\text{ox}} + \frac{1}{2} E_{\text{s}} \cdot x_{\text{do}} = \frac{qN_{\text{a}} x_{\text{do}}}{\epsilon_{\text{ox}}} \cdot t_{\text{ox}} + \frac{qN_{\text{a}}}{2\epsilon_{\text{s}}} x_{\text{do}}^2\end{aligned}$$

Define oxide capacitance $C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$. x_{do} can be solved from above equation:

$$x_{\text{do}} = \frac{\epsilon_{\text{s}}}{C_{\text{ox}}} \left(\sqrt{1 + \frac{2C_{\text{ox}}\phi_{\text{B}}}{\epsilon_{\text{s}} q N_{\text{a}}}} - 1 \right)$$

Si surface potential:

$$\phi(0) = \phi_{\text{s}} = \phi_{\text{p}} + \frac{1}{2} \frac{qN_{\text{a}}}{\epsilon_{\text{s}}} x_{\text{do}}^2$$

This is very important to calculate $n(0), p(0)$ carrier concentration at the surface!!
Now we see that x_{do} should be less than x_{po} in the n$^+$p junction case, because much less potential drop ($V_{\text{B,O}}$ compared to ϕ_{B}) a lot of potential dropped across the oxide.

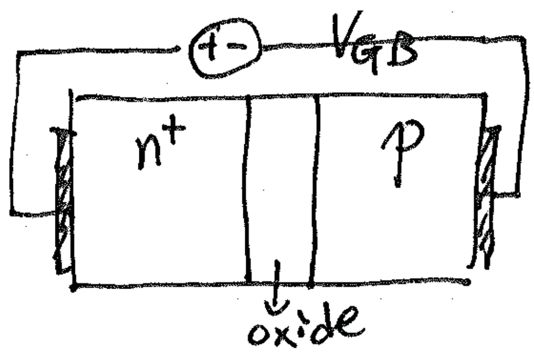
Now let us do some calculation: n^+-polysilicon gate, $10^{20}\,\text{cm}^{-3}$ and p-type substrate $N_A = 10^{17}\,\text{cm}^{-3}$.

$$
\begin{aligned}
t_{ox} &= 100\,\text{A} = 10\,\text{nm} = 1\times10^{-6}\,\text{cm} \\
x_{do} &= \text{?} \quad \text{surface carrier concentration } n(0), p(0) \\
C_{ox} &= \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\times8.85\times10^{-14}\,\text{F/cm}}{1\times10^{-6}\,\text{cm}} = 3.45\times10^{-7}\,\text{F/cm}^2 \quad \text{capacitance per unit area} \\
\phi_B &= \phi_{n^+} - \phi_p = 550\,\text{mV} - (-420\,\text{mV}) = 970\,\text{mV} = 0.97\,\text{V} \\
x_{do} &= \frac{\epsilon_s}{C_{ox}}\left(\sqrt{1+\frac{2C_{ox}^2\phi_B}{\epsilon_s q N_a}}-1\right) \\
&= \frac{11.9\times8.85\times10^{-14}\,\text{Fcm}^{-1}}{3.45\times10^{-7}\,\text{Fcm}^{-2}}\left(\sqrt{1+\frac{2\times(3.45\times10^{-7})^2\times(0.97\,\text{V})\,\text{F}^2/\text{cm}^4}{11.7\times8.85\times10^{-14}\times1.6\times10^{-19}\times10^{17}\,\text{cm}^{-3}}}-1\right) \\
&= 2.98\times10^{-6}\,\text{cm}\cdot\left(\sqrt{1+\frac{2\times0.97}{8.85\times1.6\times10^{-2}}}-1\right) \\
&= 2.98\times10^{-6}\,\text{cm}\,\times(3.83-1) = 8.45\times10^{-6}\,\text{cm} = 84.5\,\text{nm} = 845\,\text{Å}
\end{aligned}
$$

On the contrary, if there is no oxide:

$$
\begin{aligned}
x_{po} &= \sqrt{\frac{2\epsilon_s\phi_B}{qN_a}} = \sqrt{\frac{2\times11.7\times8.85\times10^{-14}\,\text{F}\cdot\text{cm}^{-1}\times0.97}{1.6\times10^{-19}\times1\times10^{17}}} = 11.2\times10^{-6}\,\text{cm} = 112\,\text{nm} \\
\phi(0) &= \phi_s = \phi_p + \frac{1}{2}\frac{qN_a}{\epsilon_s}x_{do}^2 = -420\,\text{mV} + \frac{1}{2}\frac{1.6\times10^{-19}\,\text{C}\times1\times10^{17}\,\text{cm}^{-3}}{11.7\times8.85\times10^{-14},\text{F}\cdot\text{cm}^{-1}}\text{times}(8.45\times10^{-6})^2 \\
&= -0.42+0.55 = 0.13\,\text{V} \\
n(0) &= n_i e^{(q\phi(0)/kT)} = 10^{10}\cdot10^{130\,\text{mV}/60\,\text{mV}} = 1.46\times10^{12}\,\text{cm}^{-3} \\
p(0) &= \frac{n_i^2}{n(0)} = 6.85\times10^{7}\,\text{cm}^{-3}
\end{aligned}
$$

Yesterday, we also talked about what happens when we apply a bias (voltage)
V_{GB} means body ground, gate in reference to body (Compare to V_D in diode case). It does not matter whether n or p for this definition. Since there is oxide, no matter $V_{GB} > 0$ or



$V_{GB} < 0$, there is no current. $\Longrightarrow$ still consider like "thermal equilibrium"

$$n(0) = n_i e^{(q\phi(0)/kT)}$$

Tomorrow, we will see more detailed discussion on what will happen to the surface carrier density $n(0)$ or $p(0)$ when we apply V_{GB}. The surface carrier density will determine whether the MOSFET channel can conduct or not.

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