

Lecture 13

Digital Circuits (III)

CMOS CIRCUITS

Outline

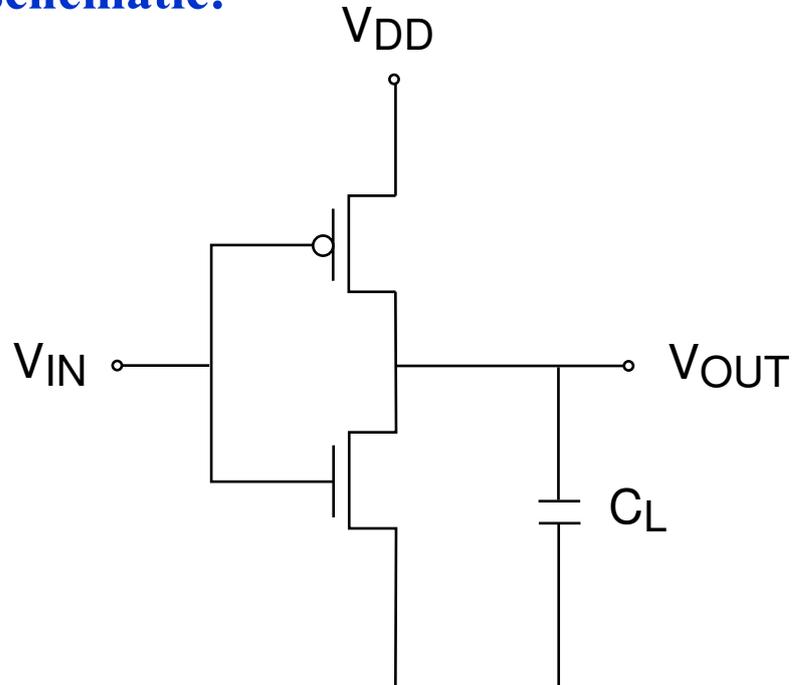
- CMOS Inverter: **Propagation Delay**
- CMOS Inverter: **Power Dissipation**
- CMOS: **Static Logic Gates**

Reading Assignment:

Howe and Sodini; Chapter 5, Sections 5.4 & 5.5

1. Complementary MOS (CMOS) Inverter

Circuit schematic:



Basic Operation:

- $V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD}$
 - $V_{GSn} = 0 (< V_{Tn}) \Rightarrow$ **NMOS OFF**
 - $V_{SGp} = V_{DD} (> -V_{Tp}) \Rightarrow$ **PMOS ON**
- $V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0$
 - $V_{GSn} = V_{DD} (> V_{Tn}) \Rightarrow$ **NMOS ON**
 - $V_{SGp} = 0 (< -V_{Tp}) \Rightarrow$ **PMOS OFF**

No power consumption while idle in any logic state!

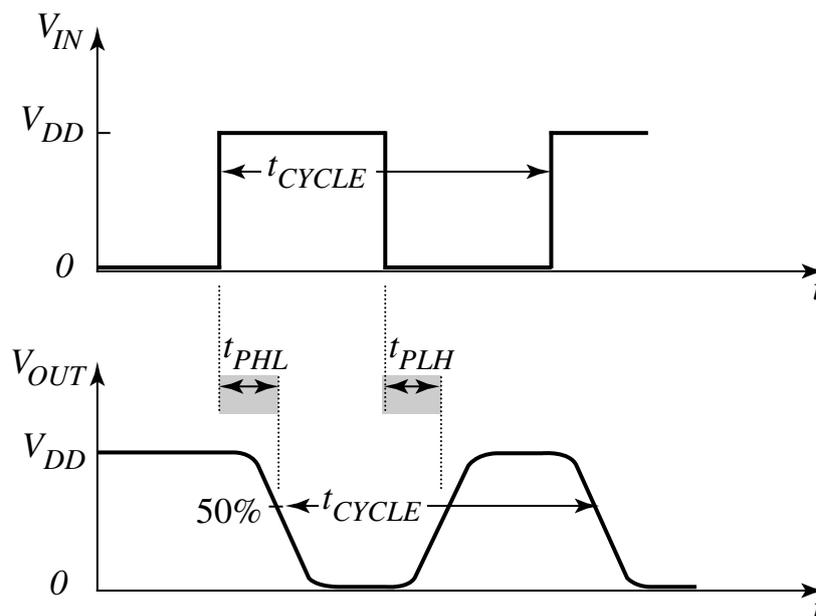
2. CMOS inverter: Propagation delay

Inverter propagation delay: time delay between input and output signals; figure of merit of logic speed.

Typical propagation delays: < 100 ps.

□ Complex logic system has 10-50 propagation delays per clock cycle.

Estimation of t_p : use square-wave at input

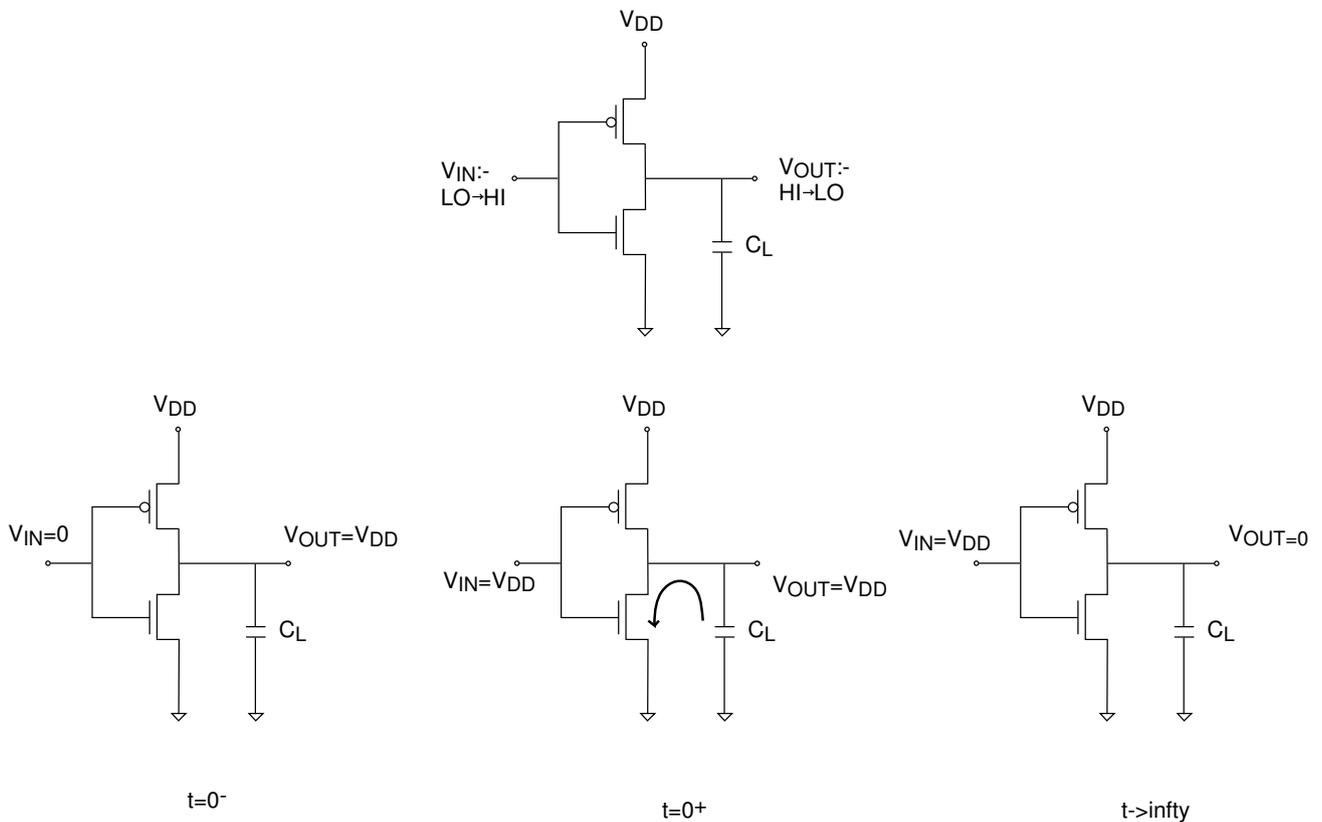


Average propagation delay:

$$t_p = \frac{1}{2} (t_{PHL} + t_{PLH})$$

CMOS inverter:

Propagation delay high-to-low



During early phases of discharge, NMOS is saturated and PMOS is cut-off.

Time to discharge *half* of charge stored in C_L :

□

$$t_{pHL} \approx \frac{\frac{1}{2} \text{ charge on } C_L \text{ @ } t = 0^-}{\text{NMOS discharge current}}$$

CMOS inverter:

Propagation delay high-to-low (contd.)

Charge in C_L at $t=0^-$:

$$Q_L(t = 0^-) = C_L V_{DD}$$

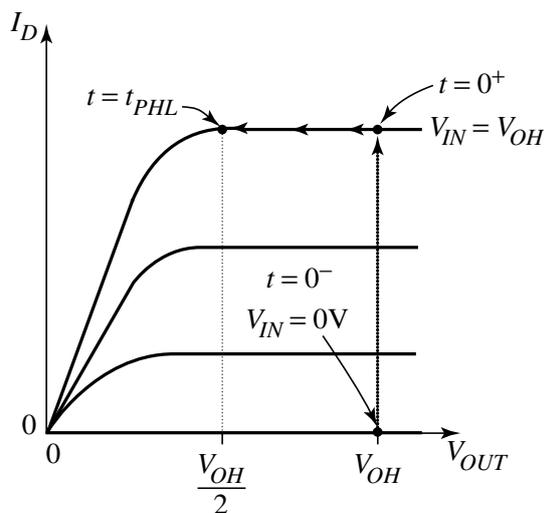
Discharge Current (NMOS in saturation):

$$I_{Dn} = \frac{W_n}{2L_n} \mu_n C_{ox} (V_{DD} - V_{Tn})^2$$

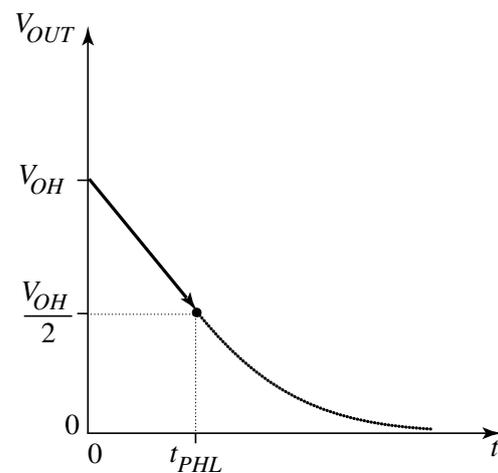
Then:

$$t_{PHL} \approx \frac{C_L V_{DD}}{\frac{W_n}{L_n} \mu_n C_{ox} (V_{DD} - V_{Tn})^2}$$

Graphical Interpretation



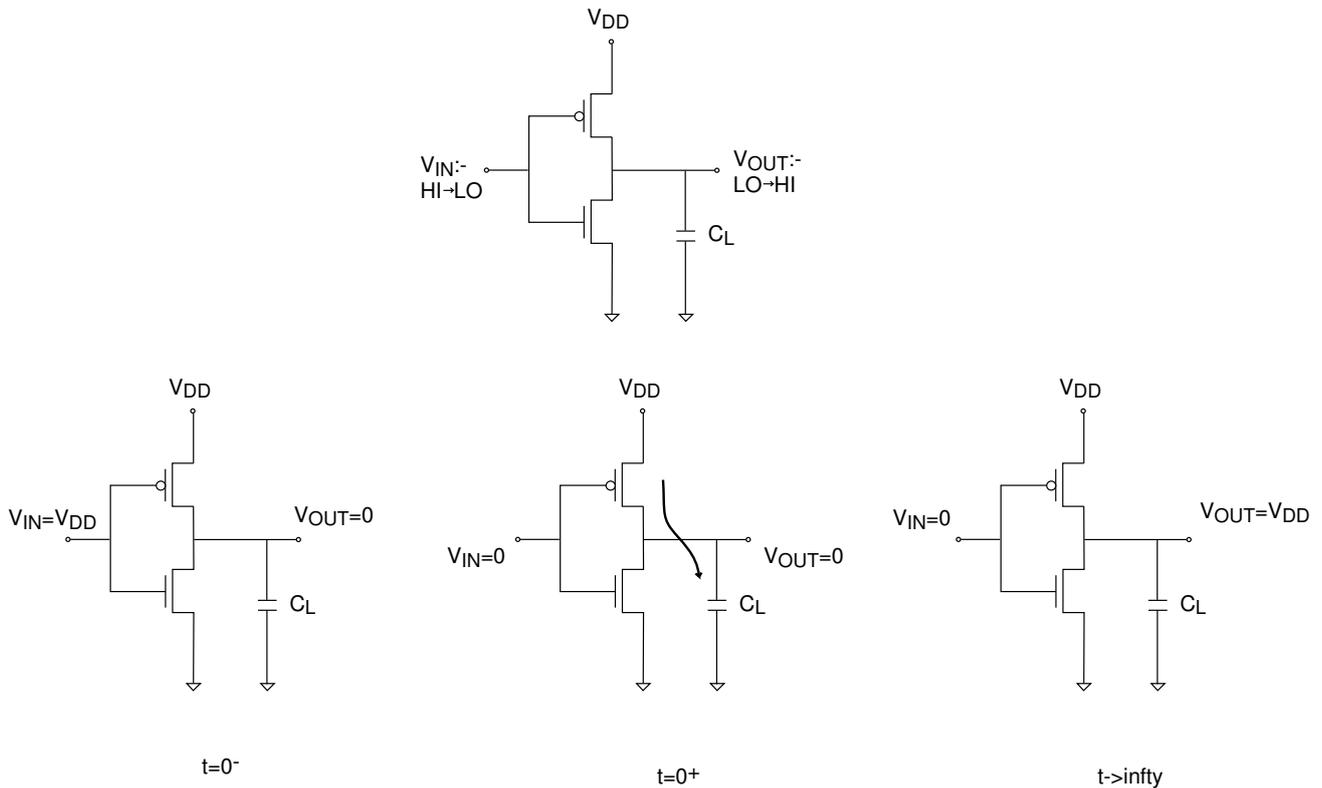
(a)



(b)

CMOS inverter:

Propagation delay low-to-high



During early phases of discharge, PMOS is saturated and NMOS is cut-off.

Time to charge to *half* of final charge on C_L :

□

$$t_{PLH} \approx \frac{\frac{1}{2} \text{ charge on } C_L \text{ @ } t = \infty}{\text{PMOS charge current}}$$

CMOS inverter:

Propagation delay high-to-low (contd.)

Charge in C_L at $t=\infty$:

$$Q_L(t = \infty) = C_L V_{DD}$$

Charge Current (PMOS in saturation):

$$-I_{Dp} = \frac{W_p}{2L_p} \mu_p C_{ox} (V_{DD} + V_{Tp})^2$$

Then:

$$t_{PLH} \approx \frac{C_L V_{DD}}{\frac{W_p}{L_p} \mu_p C_{ox} (V_{DD} + V_{Tp})^2}$$

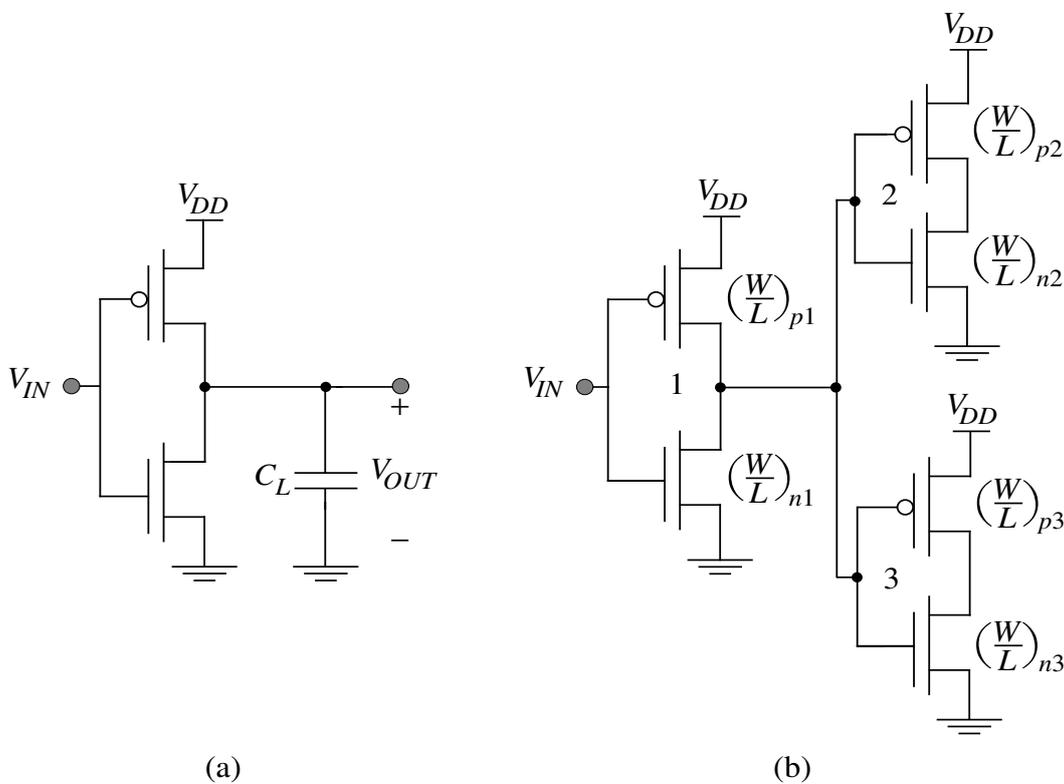
Key dependencies of propagation delay:

- $V_{DD} \uparrow \Rightarrow t_p \downarrow$
 - Reason: $V_{DD} \uparrow \Rightarrow Q(C_L) \uparrow$, but I_D goes as square \uparrow
 - Trade-off: $V_{DD} \uparrow \Rightarrow$ more power consumed.
- $L \downarrow \Rightarrow t_p \downarrow$
 - Reason: $L \downarrow \Rightarrow I_D \uparrow$
 - Trade-off: manufacturing cost!

Components of load capacitance C_L :

- *Following logic gates*: must add capacitance of each gate of every transistor the output is connected to.
- *Interconnect wires* that connects output to input of following logic gates
- *Own drain-to-body capacitances*

$$C_L = C_G + C_{\text{wire}} + C_{\text{DBn}} + C_{\text{DBp}}$$



Gate Capacitance of Next Stage

- Estimation of the input capacitance:
 - n- and p-channel transistors in the next stage switch from triode through saturation to cutoff during a high-low or low-high transition
- Requires nonlinear charge storage elements to accurately model
- Hand Calculation use a **rough estimate** for an inverter

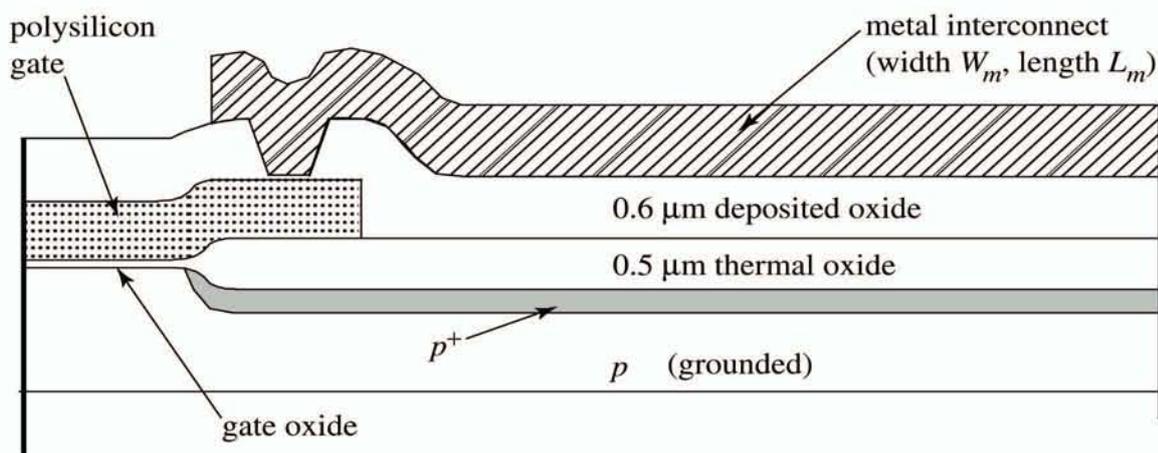
$$C_{in} = C_{ox}(WL)_p + C_{ox}(WL)_n$$

CG for example circuit

$$C_G = C_{ox}(WL)_{p2} + C_{ox}(WL)_{n2} + \\ C_{ox}(WL)_{p3} + C_{ox}(WL)_{n3}$$

Interconnect Capacitance

- “Wires” consist of metal lines connecting the output of the inverter to the input of the next stage



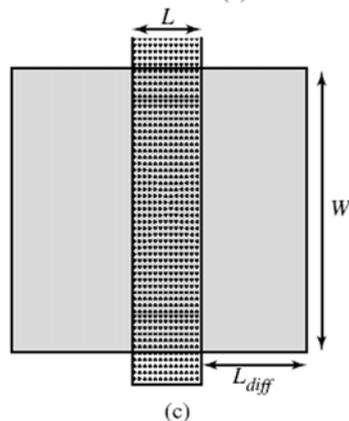
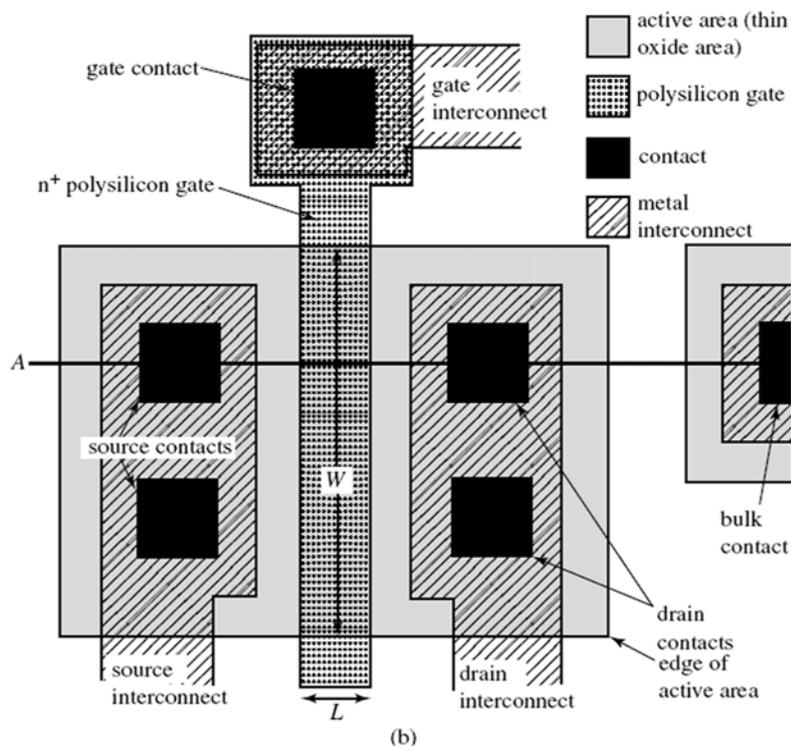
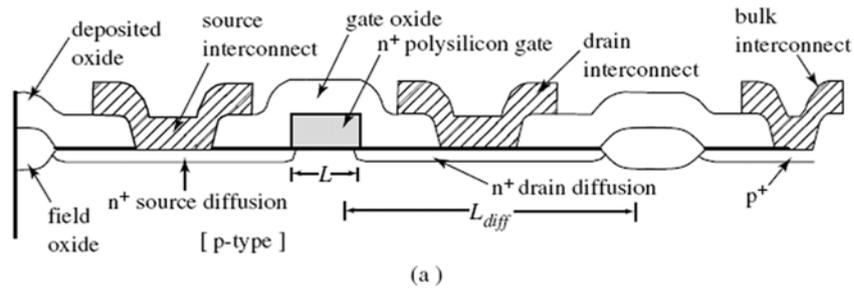
- The p^+ layer (i.e., heavily doped with acceptors) under the thick thermal oxide (500 nm = 0.5 μm) and deposited oxide (600 nm = 0.6 μm) depletes only slightly when positive voltages appear on the metal line, so the capacitance is approximately the oxide capacitance:

$$C_{\text{wire}} = C_{\text{thickox}} (W_m * L_m)$$

where the oxide thickness = 500 nm + 600 nm = 1.1 μm .

For large digital systems, the **parasitic wiring capacitance** can **dominate** the load capacitance

Parasitic Capacitance-Drain/Bulk Depletion



Calculation of Parasitic Drain/Bulk Junction Depletion Capacitance

- Depletion $q_J(v_D)$ is non-linear --> take the worst case and use the zero-bias capacitance C_{j0} as a linear charge-storage element during the transient.
- “Bottom” of depletion regions of the inverter’s drain diffusions contribute a depletion capacitance:

$$C_{JBOT} = C_{Jn}(W_n L_{diffn}) + C_{Jp}(W_p L_{diffp})$$

Where: C_{Jn} and C_{Jp} are the zero-bias bottom capacitance ($\text{fF}/\mu\text{m}^2$) for the n-channel and p-channel MOSFET drain-bulk junction, respectively.

Typical numbers: C_{Jn} and C_{Jp} are about $0.2 \text{ fF}/\mu\text{m}^2$

- “Sidewall” of depletion regions of the inverter’s drain diffusions make an additional contribution:

$$C_{JSW} = (W_n + 2L_{diffn})C_{JSWn} + (W_p + 2L_{diffp})C_{JSWp}$$

Where: C_{JSWn} and C_{JSWp} are the zero-bias sidewall capacitance ($\text{fF}/\mu\text{m}$) for the n-channel and p-channel MOSFET drain-bulk junction, respectively.

Typical numbers: C_{JSWn} and C_{JSWp} are about $0.5 \text{ fF}/\mu\text{m}$

The sum of C_{JBOT} and C_{JSW} is the total depletion capacitance, C_{DB}

Power Dissipation

- Energy from power supply needed to charge up the capacitor:

$$E_{charge} = \int V_{DD} i(t) dt = V_{DD} Q = V_{DD}^2 C_L$$

- Energy stored in capacitor:

$$E_{store} = 1/2 C_L V_{DD}^2$$

- Energy lost in p-channel MOSFET during charging:

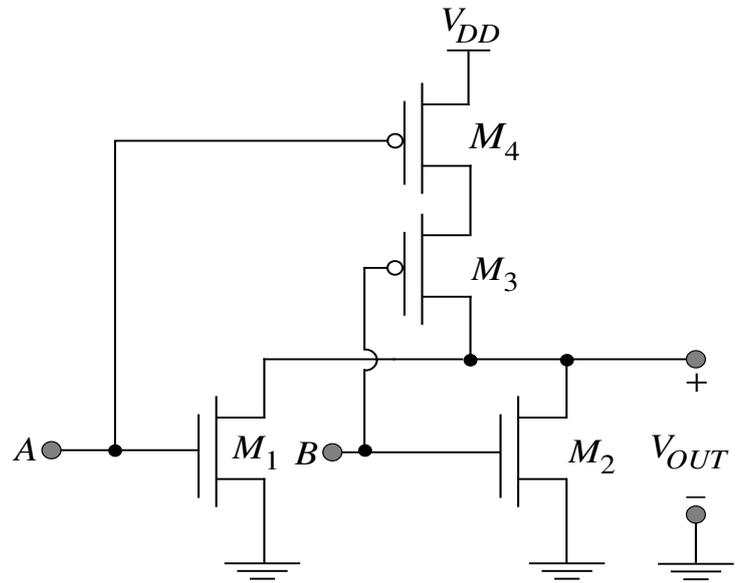
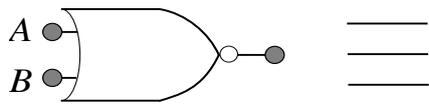
$$E_{diss} = E_{charge} - E_{store} = 1/2 C_L V_{DD}^2$$

- During discharge the n-channel MOSFET dissipates an identical amount of energy.
- If the charge/discharge cycle is repeated f times/second, where f is the clock frequency, the **dynamic power dissipation** is:

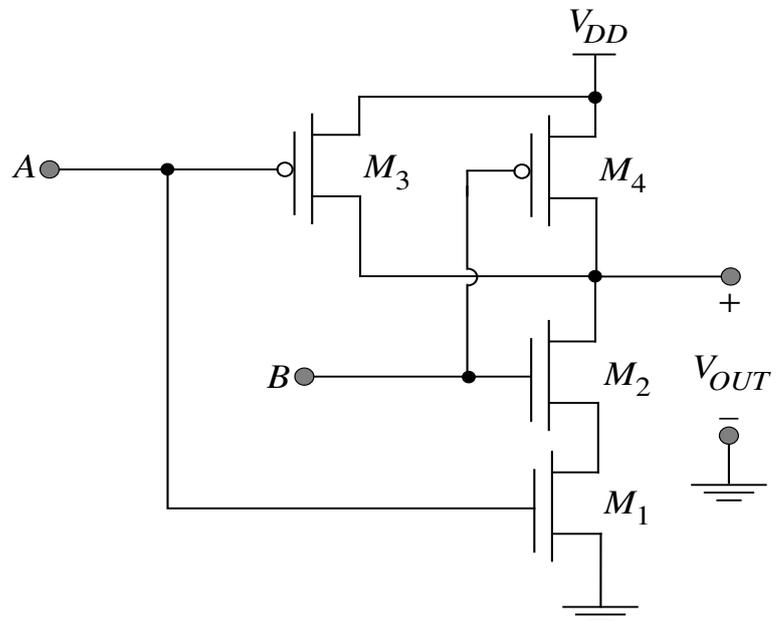
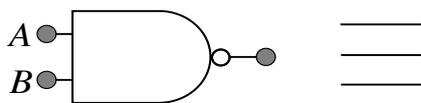
$$P = 2E_{diss} * f = C_L V_{DD}^2 f$$

In practice many gates do not change state every clock cycle which lowers the power dissipation.

CMOS Static Logic Gates



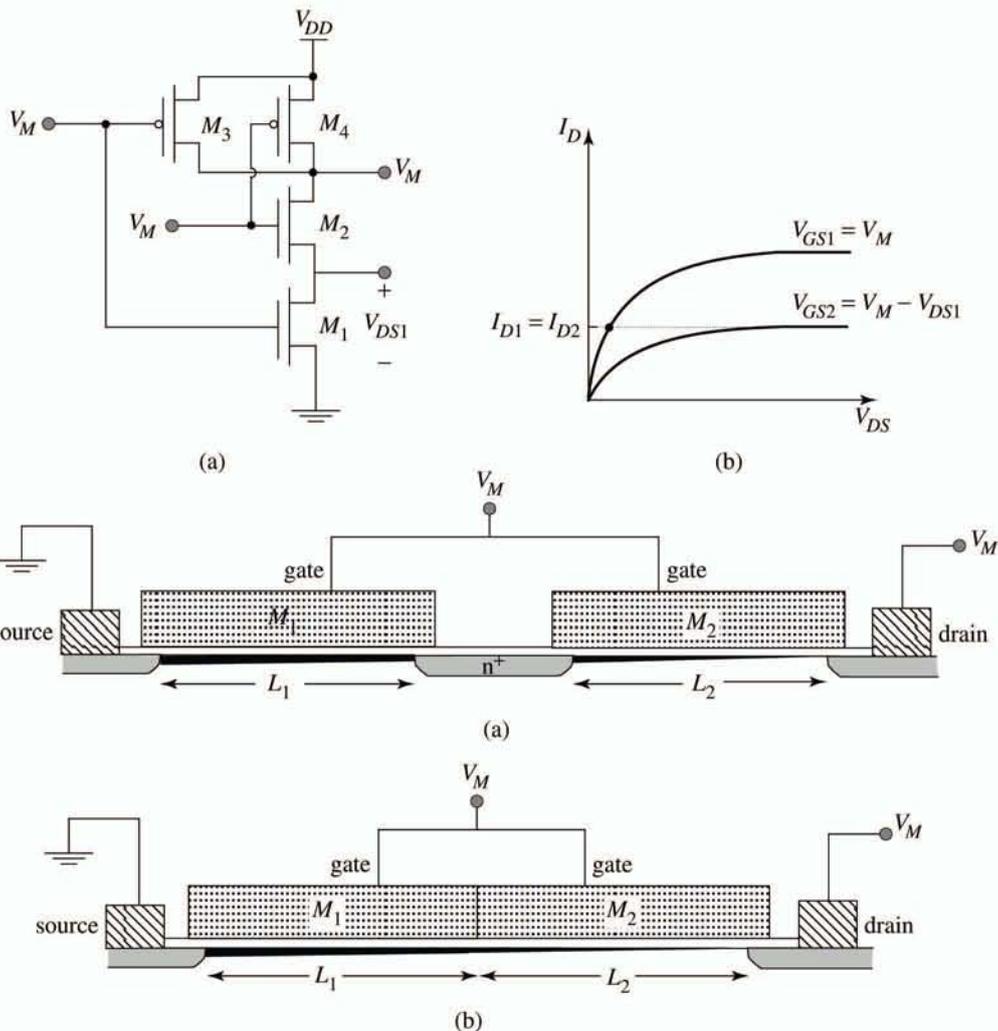
(a)



(b)

CMOS NAND Gate

I-V Characteristics of n-channel devices



- Effective length of two n-channel devices is $2L_n$
 - $k_{neff} = k_{n1}/2 = k_{n2}/2$ Recall $k_n = W/L\mu_n C_{ox}$
- Effective width of two p-channel devices is $2W_p$ BUT worst case only one device is on
 - $k_{peff} = k_{p3} = k_{p4}$

Calculation of static and transient performance for NAND Gate

- $k_{peff} = k_{neff}$ is desirable for equal propagation delays and symmetrical transfer characteristics
- Recall $\mu_n = 2\mu_p$
- Therefore $(W/L)_n = (W/L)_p$
for 2-input NAND gate
- In general for an M-input NAND Gate

$$\left(\frac{W}{L}\right)_n = \frac{M}{2} \left(\frac{W}{L}\right)_p$$

What did we learn today?

Summary of Key Concepts

Key features of CMOS inverter:

- No current between power supply and ground while inverter is idle in any logic state
- “rail-to-rail” logic
 - Logic levels are 0 and V_{DD} .
- High $|A_v|$ around the logic threshold
 - \Rightarrow Good noise margins.

CMOS inverter logic threshold and noise margins engineered through W_n/L_n and W_p/L_p .

Key dependencies of propagation delay:

- $V_{DD} \uparrow \Rightarrow t_p \downarrow$
- $L \downarrow \Rightarrow t_p \downarrow$

Power dissipation CV^2f

Sizing static gates

MIT OpenCourseWare
<http://ocw.mit.edu>

6.012 Microelectronic Devices and Circuits
Spring 2009

For information about citing these materials or our Terms of Use, visit: <http://ocw.mit.edu/terms>.