6.012 Microelectronic Devices and Circuits
Spring 2005

March 9, 2005
Quiz #1

Problem #points

NAME________________________________ 1__________

RECITATION TIME________________________ 2__________

3__________

Total____________

General guidelines (please read carefully before starting):

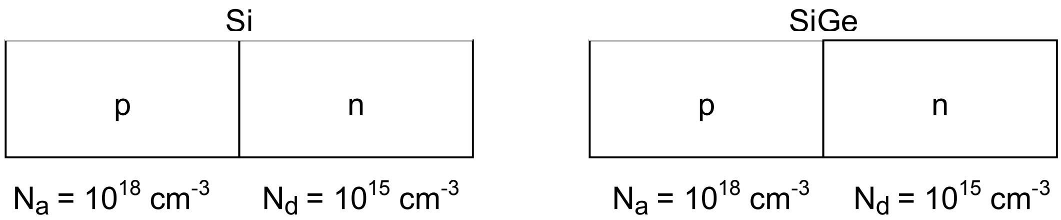
- Make sure to write your name on the space provided above.
- Open book: you can use any material you wish. But no computers.
- All answers should be given in the space provided. Please do not turn in any extra material.
- You have 120 minutes to complete the quiz.
- Make reasonable approximations and *state them*, i.e. low-level injection, extrinsic semiconductor, quasi-neutrality, etc.
- Partial credit will be given for setting up problems without calculations. NO credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. N_a, τ, ε, etc.
- Pay attention to problems in which *numerical answers* are expected. An algebraic answer will not accrue full points. Every numerical answer must have the proper *units* next to it. Points will be subtracted for answers without units or with wrong units. In situations with a defined axis, the *sign* of the result is also part of the answer.

Unless otherwise stated, use:

$q = 1.6 \times 10^{-19}$ C
$kT/q = 25$ mV at room temperature
$n_i = 10^{10}$ cm^{-3} for silicon at room temperature
$\varepsilon_{si} = 10^{-12}$ F/cm $\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm

1. (30 points)

Consider two pn-junction diodes that have identical uniform doping profiles, but differ in substrate – one is made of silicon, and one is made of a silicon-germanium alloy (SiGe). Assume the intrinsic carrier concentration for SiGe at room temperature is approximately 10^{13} cm^{-3} and $\varepsilon_{SiGe} = 1.5 \times 10^{-12}$ F/cm



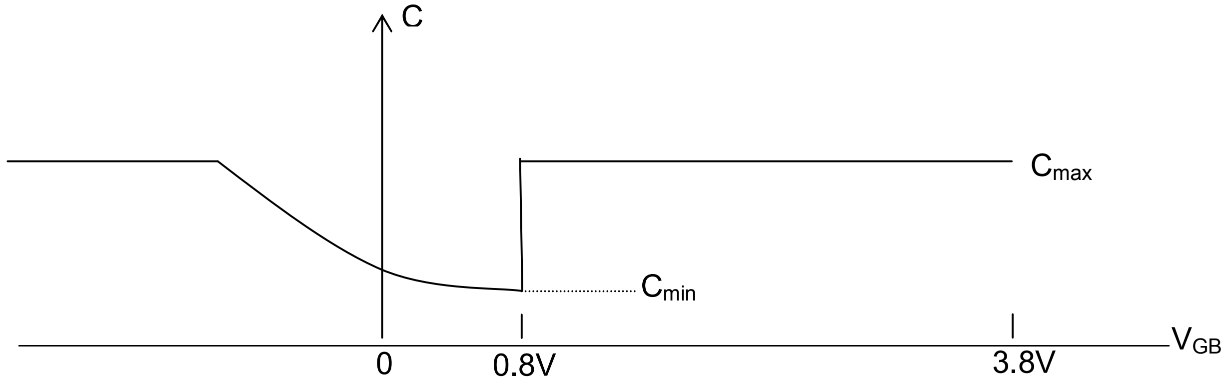
a) Calculate the built in potential for both the silicon and SiGe diodes.

b) Calculate the ratio of the depletion width on the n-side of the two diodes x_{no} in thermal equilibrium. [i.e. x_{no}(Si)/ x_{no}(SiGe)]

c) Calculate the ratio of the electric fields at the metallurgical junction of the two diodes in thermal equilibrium. [i.e. E_o(Si)/E_o(SiGe)]

2. (35 Points)

An n^+ polysilicon gate ($N_d > 10^{20}$ cm^{-3}) MOS capacitor with p-type Si body has a capacitance-voltage plot shown below. The maximum capacitance per unit area $C_{max} = 1.7 \times 10^{-7}$ F/cm^2, while the minimum capacitance per unit area $C_{min} = 6.2 \times 10^{-8}$ F/cm^2. Assume $\phi_{n^+} = 0.55$ V.



a) What region of operation is the device in for V_{GB} = 3.8V?

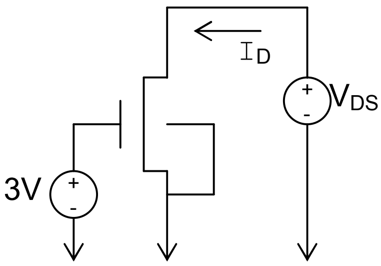
b) For the device in part (a), derive an expression for the depletion region width x_d at V_{GB} = 3.8V, in terms of C_{min} and C_{max} and fundamental parameters (e.g. q, ε_{ox}, ε_s, etc.)

c) For the device in part (a), if the magnitude of the gate charge $|Q_G| = 6.74 \times 10^{-7}$ C/cm^2, at V_{GB} = 3.8V, derive an expression for the doping N_a, in terms of C_{min}, C_{max} and other fundamental parameters.

d) Calculate N_a from part (c) assuming $|Q_G| = 6.74 \times 10^{-7}$ C/cm^2 and the other parameters given in (a) above:

3. (35 points)

You are given an MOS transistor with the device parameters shown below.



$W = 10 \mu m$

$C_{OX} = 10^{-7}\ F/cm^2$

$\mu_n = 200\ cm^2/V\text{-}s$

$V_{Tn} = 1V$

A drain-to-source voltage is applied resulting in the electric field at the source $E_y\ (0) = -3.75 \times 10^3$ V/cm and at the drain $E_y(L) = -7.5 \times 10^3$ V/cm

a) Calculate I_D.

b) Calculate the V_{DS} applied.

c) Calculate the channel length L of this device.

d) What region of operation is the transistor biased? (Circle one and explain.)

Cutoff Triode Saturation

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