Lecture 23 - Circuits at High Frequencies - Outline

- **Announcements**

  Design Problem - Due tomorrow, Dec. 4, by 5 p.m.

  Postings on Stellar - Cascode; µA-741

- **Bounding mid-band - finding ω_{HI}, ω_{LO}**

  Method of open circuit time constants: finding ω_{HI} **(How high can we fly?)**

  Method of short circuit time constants: finding ω_{LO} **(How low can we go?)**

  The lesson of the OCTC and SCTC methods: which capacitors matter

- **The Miller effect: why C_μ and C_{gd} are so important**

  The concept: the consequences of having a capacitor shunting a gain stage

  Examples: common-emitter/-source stages
  common-base/gate stages; emitter-/source-followers
  the µA 741 - stabilizing a high gain circuit

- **The Marvelous cascode: impact on ω_{HI}**

  Concept and ω_{HI}: getting larger bandwidth from CE + CB

  The costs

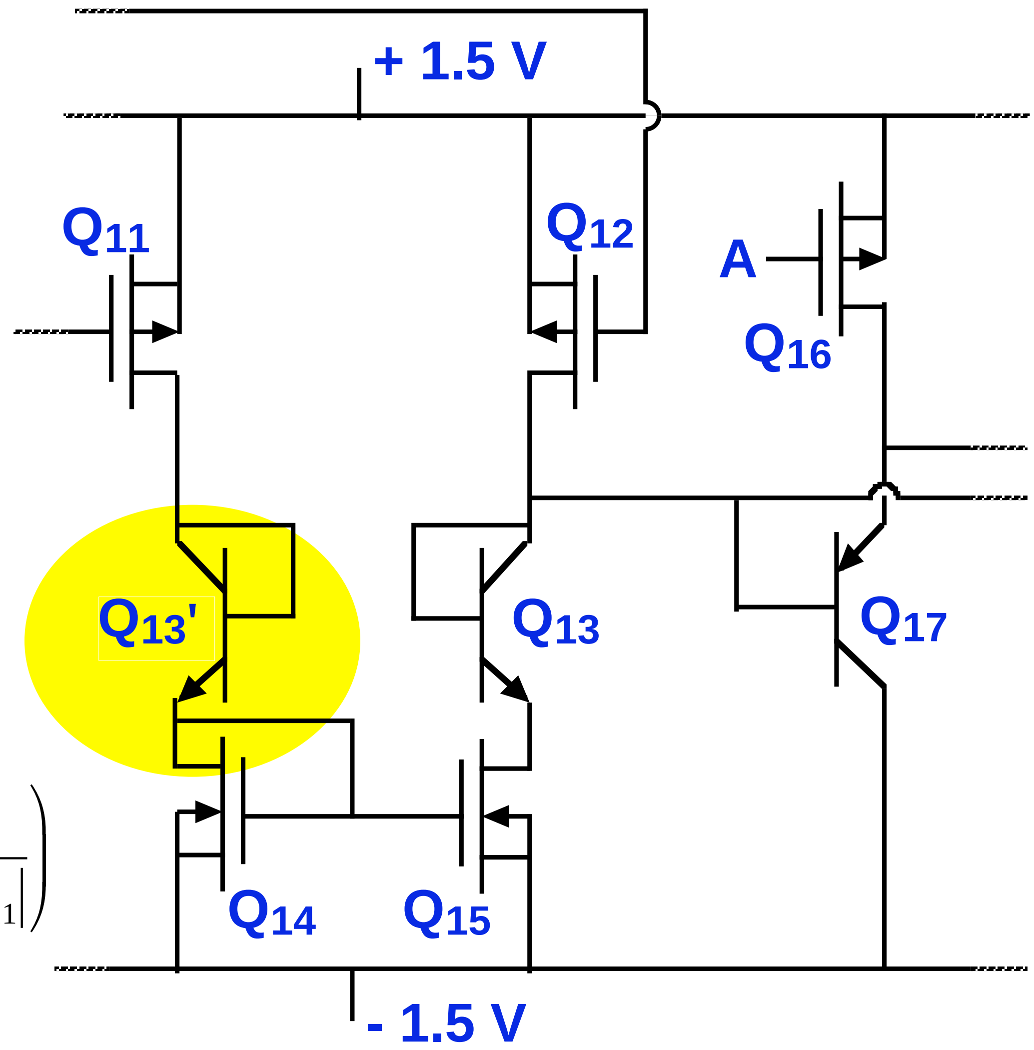
The impact of Q13' and Q13 on the voltage gains

We added transistor Q_{13} to the left side of the DP second gain stage (the Current Mirror), and said it has no effect on the A_{vd} or A_{vc} of this stage. In fact it does have some impact on the common-mode voltage gain. The following few sides look at this impact.

We find that now:

$$A_{vc} \approx \left(1 + \frac{g_{m11}}{g_{m13'}}\right) = \left(1 + \frac{2V_{thermal}}{|V_{GS11}| - |V_{T11}|}\right)$$

$$\approx 1.5$$

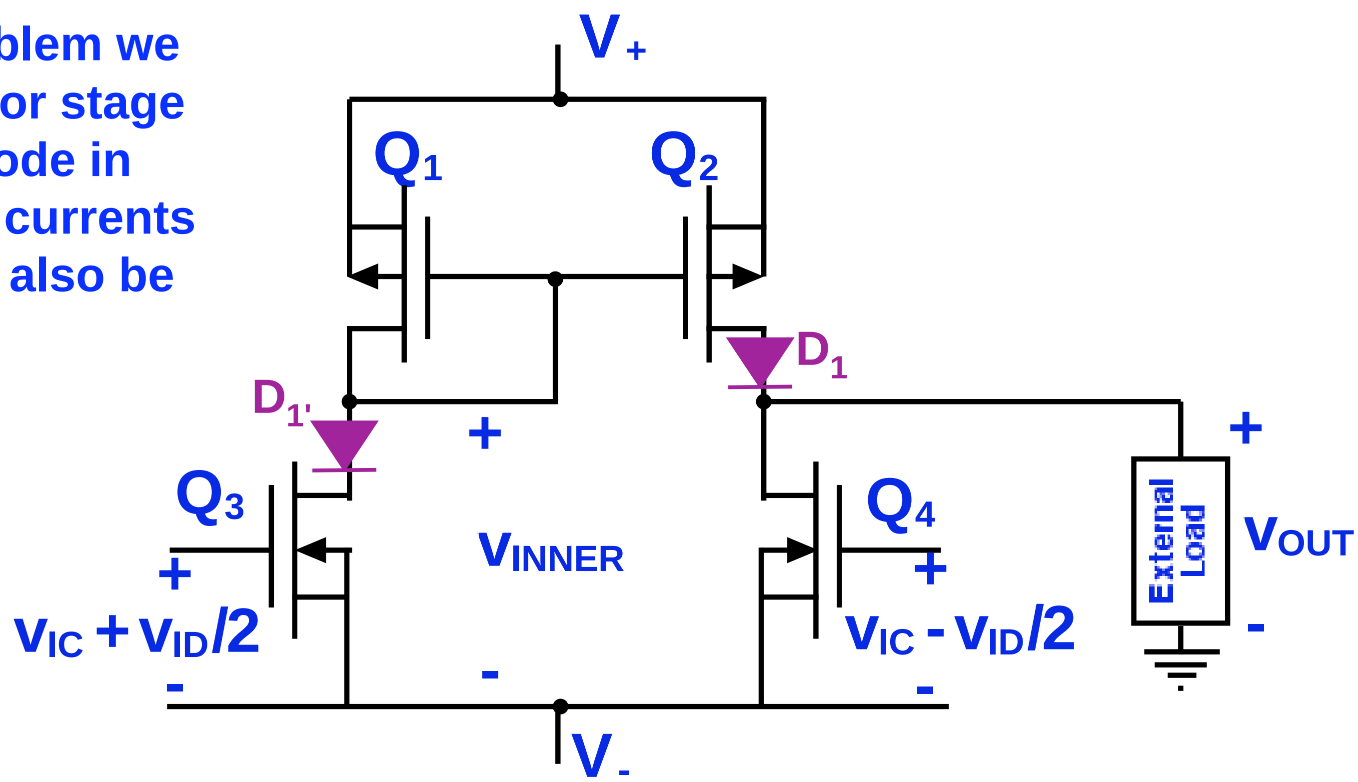


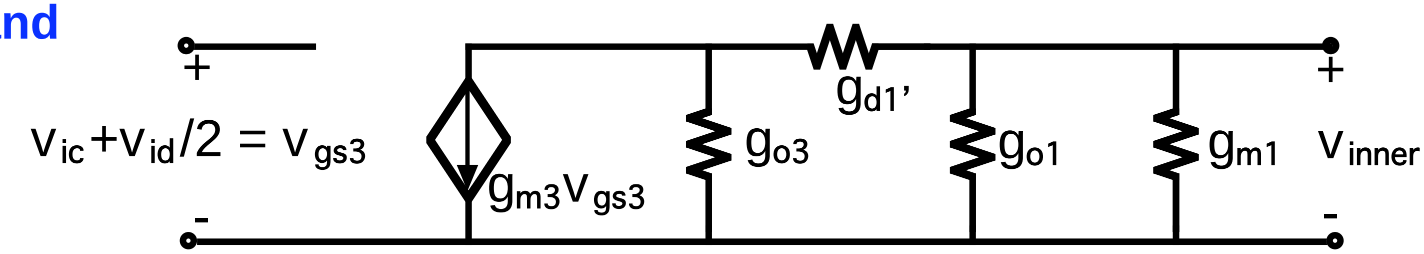
Remember that it is possible to make the bias currents in the two legs of the mirror (Q_{11}/Q_{14} and Q_{12}/Q_{15}) different by making the transistors widths different.

The impact of Q13' and Q13 on the voltage gains, cont.

In the design problem we have a current mirror stage with a level shift diode in each leg. The bias currents of the two legs can also be different.

We can do an LEC analysis of this circuit in the same way we did without the two diodes. We start with the LEC for the left side and find v_{inner}:





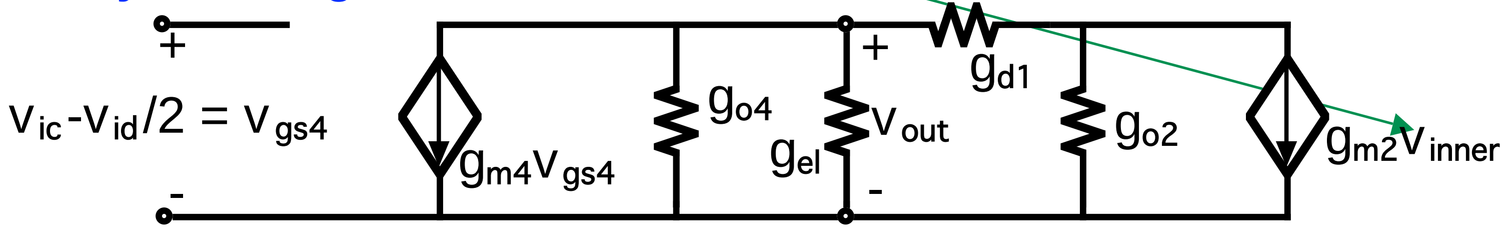
LEC for the left side

The impact of Q13' and Q13 on the voltage gains, cont.

The left side LEC gives:

$$v_{inner} \approx -(1-\delta)\left(v_{ic} + \frac{v_{id}}{2}\right) \qquad \text{with} \qquad \delta \equiv \frac{r_{d1'} + 2r_{m3}}{r_{o3}} = \frac{2g_{o3}}{g_{m3}}\left(1 + \frac{g_{m3}}{2g_{d1'}}\right)$$

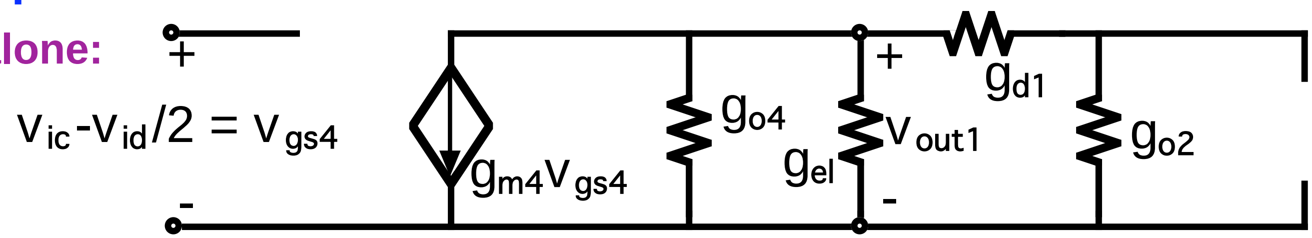
Next we analyze the right side LEC:



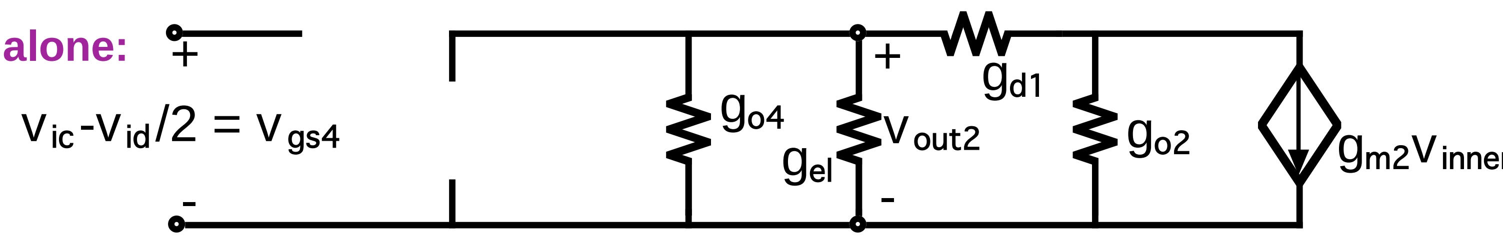
LEC for the right side

To see the impact of g_{d1} on this side, apply one source at a time and superimpose the results:

$g_{m4}v_{gs4}$ alone:



$g_{m2}v_{inner}$ alone:



The impact of Q13' and Q13 on the voltage gains, cont.

Note: Analysis sets $g_{m1} = g_{m3}$, $g_{m2} = g_{m4}$, $g_{o1} = g_{o3}$, $g_{o2} = g_{o4}$.

Writing $r_{o4}||r_{el}$ as r_{o4}^*, and doing this we find:

$$v_{out} = v_{out1} + v_{out2} = \frac{(r_{o2}+r_d)\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)} g_{m4} v_{gs4} - \frac{r_{o2}\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)}(1-\delta) g_{m2} v_{gs2}$$

$$= \frac{(r_{o2}+r_d)\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)} g_{m4}\left(v_{ic} - \frac{v_{id}}{2}\right) - \frac{r_{o2}\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)}(1-\delta) g_{m2}\left(v_{ic} + \frac{v_{id}}{2}\right)$$

Next look at the terms involving v_{id} and v_{ic} terms separately:

v_{id}:

$$-\left[\frac{(r_{o2}+r_d)\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_{el})} g_{m4} + \frac{r_{o2}\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)}(1-\delta) g_{m2}\right]\frac{v_{id}}{2} \approx \frac{r_{o2}\,r_{o4}^*(2-\delta)}{(r_{o4}^*+r_{o2}+r_d)} g_{m4}\,\frac{v_{id}}{2}$$

v_{ic}:

$$-\left[\frac{(r_{o2}+r_d)\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)} g_{m4} - \frac{r_{o2}\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)}(1-\delta) g_{m2}\right] v_{ic} = \frac{(r_d+\delta\, r_{o2})\,r_{o4}^*}{(r_{o4}^*+r_{o2}+r_d)} g_{m4}\, v_{ic}$$

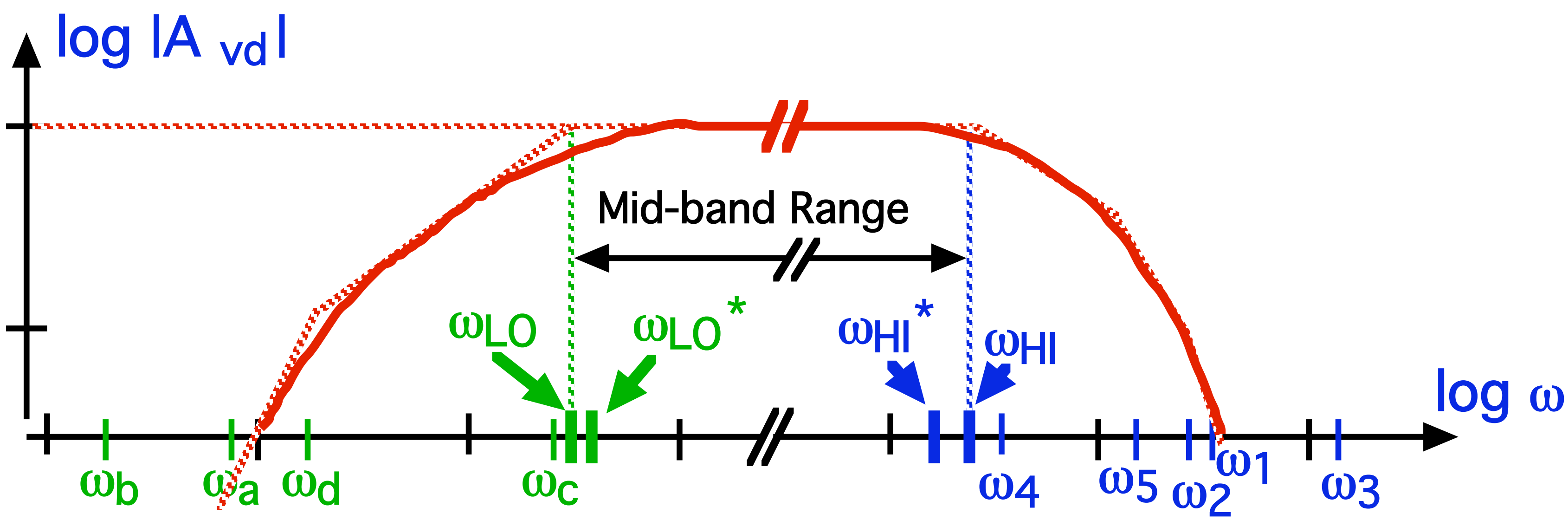
Ultimately we find:

$$v_{out} \approx \underbrace{\frac{2g_{m4}}{(2g_{o4}+g_{el})}}_{\approx\text{ unchanged by adding diodes}} \frac{(v_{in1}-v_{in2})}{2} - \underbrace{\left(1+\frac{g_{m1}}{g_{d1'}}\right)}_{\approx 1.5\text{, increased from }\approx 1\text{ by adding diodes}} \frac{(v_{in1}+v_{in2})}{2}$$

≈ unchanged by adding diodes **≈ 1.5, increased from ≈1 by adding diodes**

Mid-band, cont: **The mid-band range of frequencies**

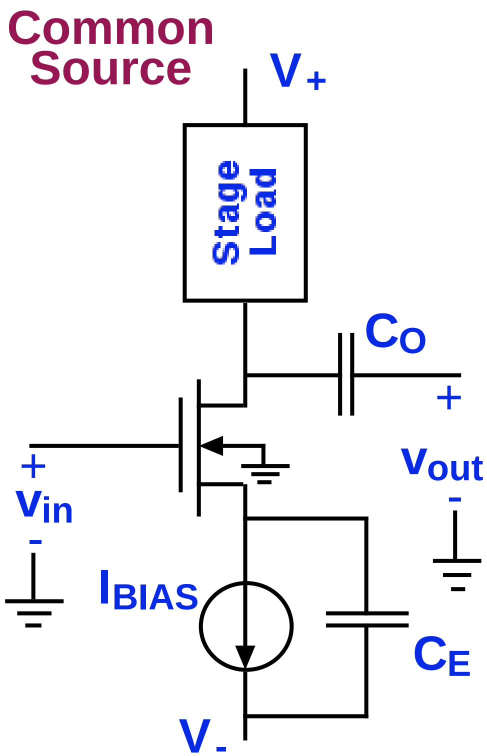
In this range of frequencies the gain is a constant, and the phase shift between the input and output is also constant (either 0˚ or 180˚).

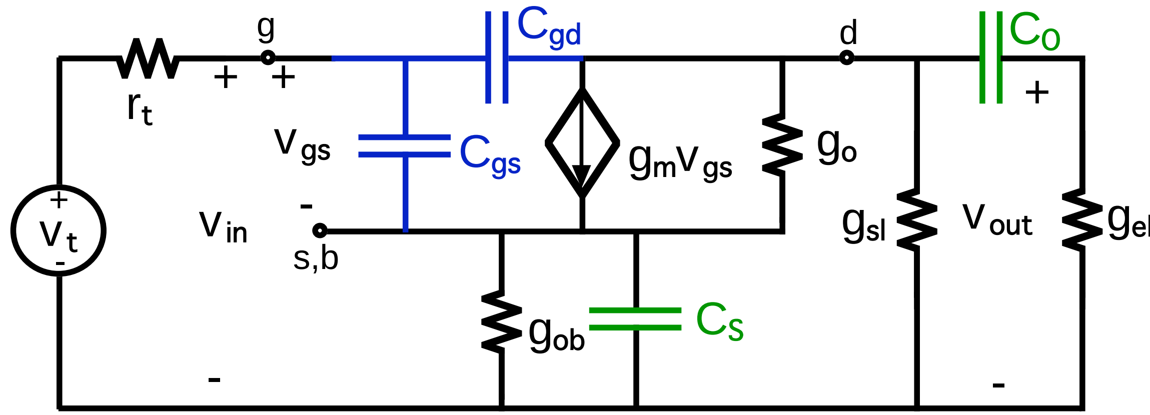


All of the <u>parasitic and intrinsic device capacitances</u> are effectively open circuits

All of the <u>biasing and coupling capacitors</u> are effectively short circuits

Bounding mid-band: frequency range of constant gain and phase



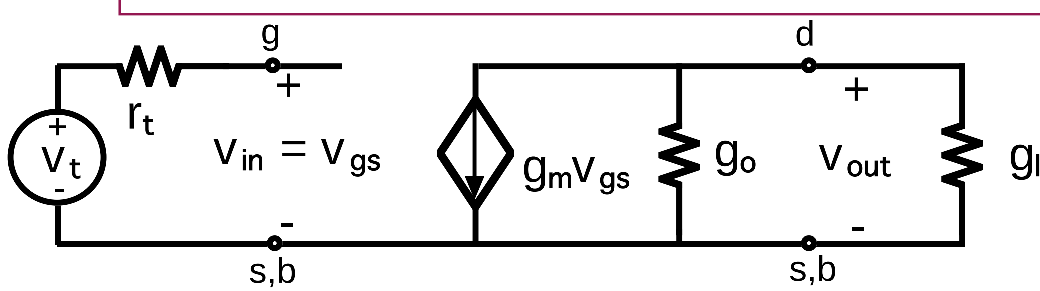


LEC for common source stage with all the capacitors

Biasing capacitors: typically in mF range
(C_O, C_S, etc.) effectively shorts above ω_{LO}

Device capacitors: typically in pF range
(C_{gs}, C_{gd}, etc.) effectively open until ω_{HI}

Mid-band frequencies fall between: $\omega_{LO} < \omega < \omega_{HI}$



Common emitter LEC for in mid-band range   Note: $g_l = g_{sl} + g_{el}$

What are ω_{LO} and ω_{HI}?

Estimating ω_{HI} - Open Circuit Time Constants Method

Open circuit time constants (OCTC) recipe:

1. Pick one C_{gd}, C_{gs}, C_μ, C_π, etc. (call it C_1) and assume all others are open circuits.
2. Find the resistance in parallel with C_1 and call it R_1.
3. Calculate $1/R_1C_1$ and call it ω_1.
4. Repeat this for each of the N different C_{gd}'s, C_{gs}'s, C_μ's, C_π's, etc., in the circuit finding $\omega_1, \omega_2, \omega_3, \ldots, \omega_N$.
5. Define ω_{HI}^* as the inverse of the sum of the inverses of the N ω_i's:

$$\omega_{HI}^* = [\Sigma(\omega_i)^{-1}]^{-1} = [\Sigma R_i C_i]^{-1}$$

6. The true ω_{HI} is similar to, but greater than, ω_{HI}^*.

Observations:

The OCTC method gives a conservative, low estimate for ω_{HI}.

The sum of inverses favors the smallest ω_i, and thus the capacitor with the largest RC product dominates ω_{HI}^*.

Estimating ω_{LO} - Short Circuit Time Constants Method

Short circuit time constants (SCTC) recipe:

1. Pick one C_O, C_I, C_E, etc. (call it C_1) and assume all others are short circuits.
2. Find the resistance in parallel with C_1 and call it R_1.
3. Calculate $1/R_1C_1$ and call it ω_1.
4. Repeat this for each of the M different C_I's, C_O's, C_E's, C_S's, etc., in the circuit finding ω_1, ω_2, ω_3, …, ω_M.
5. Define ω_{LO}* as the sum of the M ω_j's:

$$\omega_{LO}^* = [\Sigma(\omega_j)] = [\Sigma(R_jC_j)^{-1}]$$

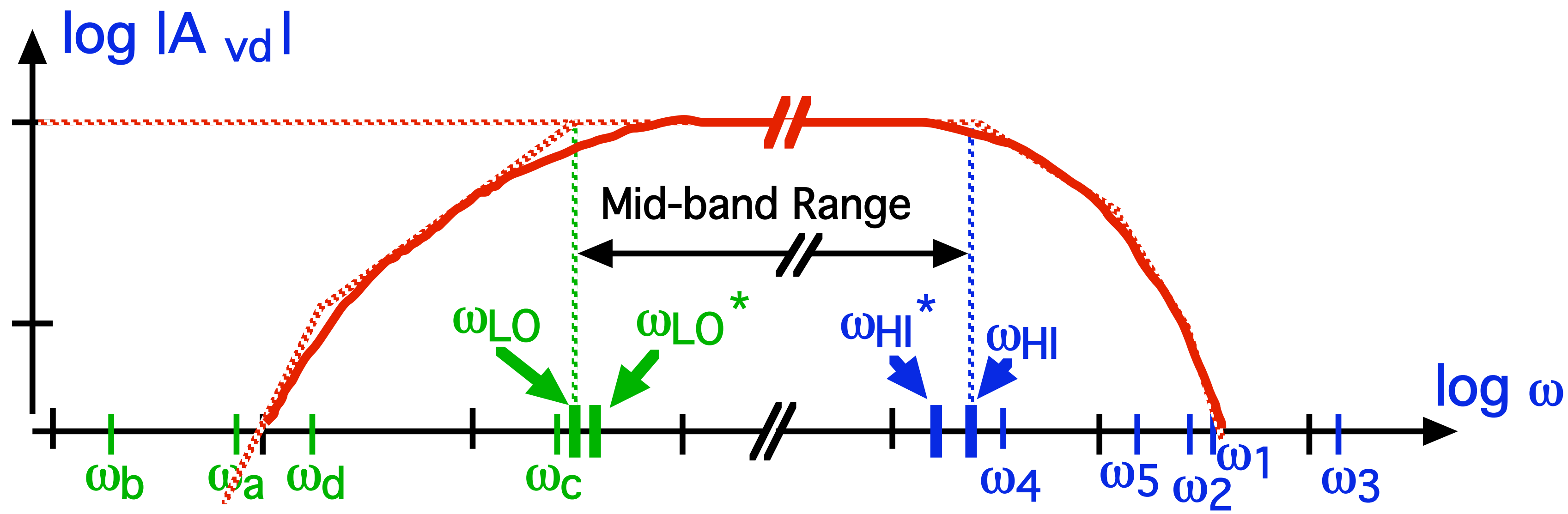
6. The true ω_{LO} is similar to, but less than, ω_{LO}*.

Observations:

The SCTC method gives a conservative, high estimate for ω_{LO}.

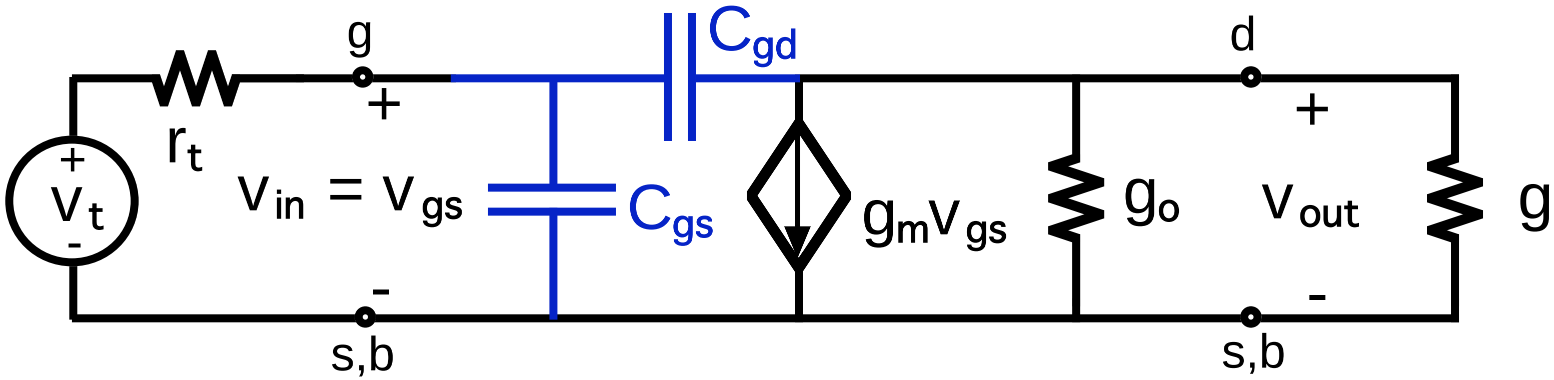
The sum of inverses favors the largest ω_j, and thus the capacitor with the smallest RC product dominates ω_{LO}*.

Summary of OCTC and SCTC results



- **OCTC:** **an estimate for ω_{HI}**
  1. **ω_{HI}* is a weighted sum of ω's associated with device capacitances: (add RC's and invert)**
  2. **Smallest ω (largest RC) dominates ω_{HI}***
  3. **Provides a lower bound on ω_{HI}**
- **SCTC:** **an estimate for ω_{LO}**
  1. **ω_{LO}* is a weighted sum of w's associated with bias capacitors: (add ω's directly)**
  2. **Largest ω (smallest RC) dominates ω_{LO}***
  3. **Provides a upper bound on ω_{LO}**

ω_{HI} for the Common Source - the full treatment



The full gain expression is:

$$A_v(j\omega) = \frac{-g_t\left(g_m - j\omega C_{gd}\right)}{\left\{(j\omega)^2 C_{gs}C_{gd} + j\omega\left[(g_l + g_o)C_{gs} + (g_l + g_o + g_t + g_m)C_{gd}\right] + (g_l + g_o)g_t\right\}}$$

There are two poles (call them ω_1 and ω_2), and one zero (call it ω_3):

$$\omega_1 = g_t \Big/ \left[C_{gs} + (g_l + g_o + g_t + g_m)\, r_l' \, C_{gd}\right] \qquad \text{with } r_l' \equiv (g_l + g_o)^{-1}$$

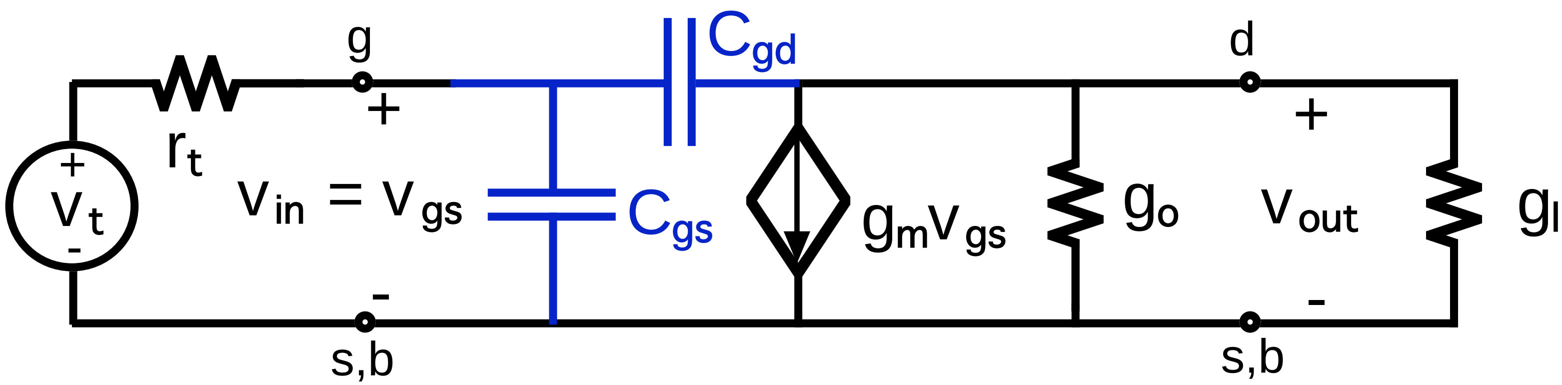
$$\omega_2 = (g_l + g_o)/C_{gd} + (g_l + g_o + g_t + g_m)/C_{gs}$$

$$\omega_3 = g_m / C_{gd}$$

Upon examination of these three expressions we find that $\omega_1 << \omega_2$, ω_3, so ω_1 is clearly the dominant pole, and ω_{HI} is effectively ω_1.

Note: C_{db} has been neglected to keep things simpler; it is very small.

ω_{HI} for the Common Source - the OCTC method



The resistance, R_{gs}, seen by C_{gs} with C_{gd} removed is $1/g_t$, so

$$\omega_{gs} = g_t / C_{gs}$$

That seen by C_{gd} with C_{gs} removed, R_{gd}, is $(g_l'+g_t+g_m)/g_t g_l'$, so

$$\omega_{gd} = g_t / \left[g_l' + g_t + g_m \right] r_l' C_{gd}$$

Using the OCTC method we estimate ω_{HI} as

$$\omega_{HI}^* = \left(\omega_{gs}^{-1} + \omega_{gd}^{-1} \right)^{-1} = g_t / \left[C_{gs} + \left(g_l' + g_t + g_m \right) r_l' C_{gd} \right]$$

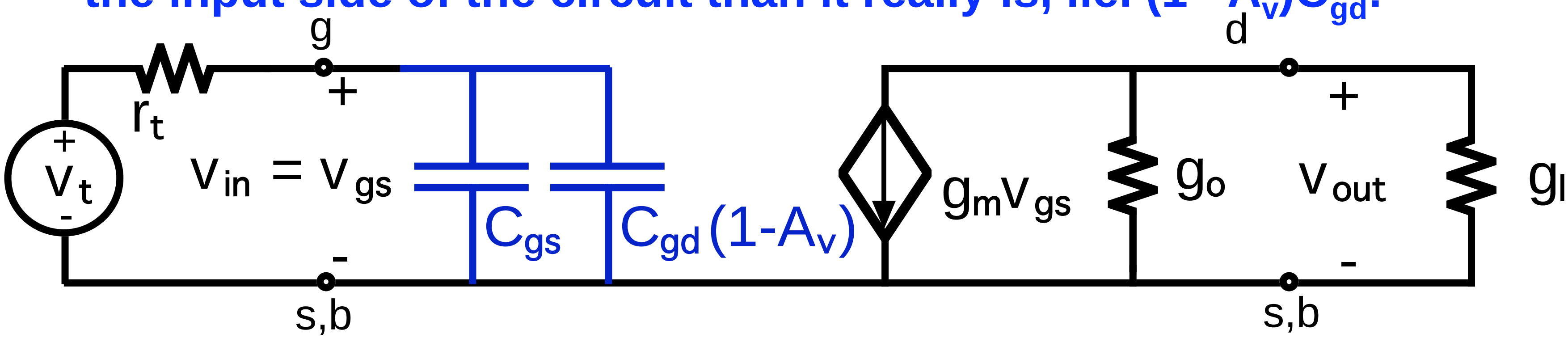
This is actually identical to the dominant pole, ω_1, found using the full analysis.

ω_{HI} for the Common Source: the Miller effect

In both of our analyses we note that in the dominant term C_{gd} is multiplied by the factor $(g_l'+g_t+g_m)r_l'$. Noting (1) that typically it is true that $g_m >> g_t$, and (2) that $-g_m r_l'$ is the mid-band voltage gain, A_v, of the amplifier, we see that this factor can be approximated as one minus the voltage gain of the stage, i.e.:

$$\left(g_l' + g_t + g_m\right)r_l' = \left[1 + \left(g_t + g_m\right)r_l'\right] \cong \left[1 + g_m r_l'\right] = \left(1 - A_v\right)$$

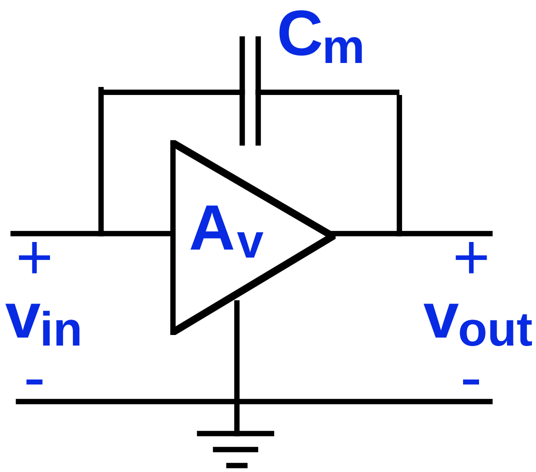
If the voltage gain is large, then in effect C_{gd} looks bigger from the input side of the circuit than it really is, i.e. $(1 - A_v)C_{gd}$:

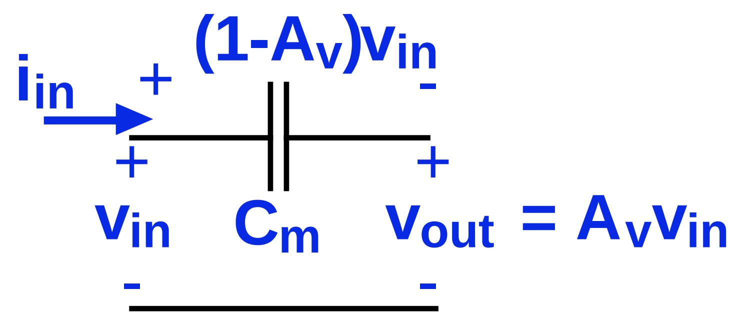


This "magnification" of a capacitor bridging the input and the output of a voltage amplifier, as C_{gd} does here, by $|A_v|$ is called the <u>Miller effect</u>.

The Miller effect (general)

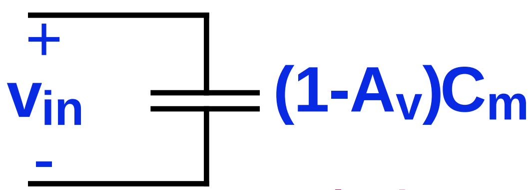
Consider an amplifier shunted by a capacitor, and consider how the capacitor looks at the input and output terminals:



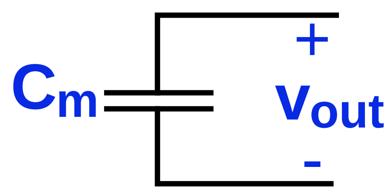


$$i_{in} = C_m \frac{d\left[(1-A_v)v_{in}\right]}{dt} = (1-A_v)C_m \frac{dv_{in}}{dt}$$

Note: A_v is negative



C_{in} looks much bigger than C_m

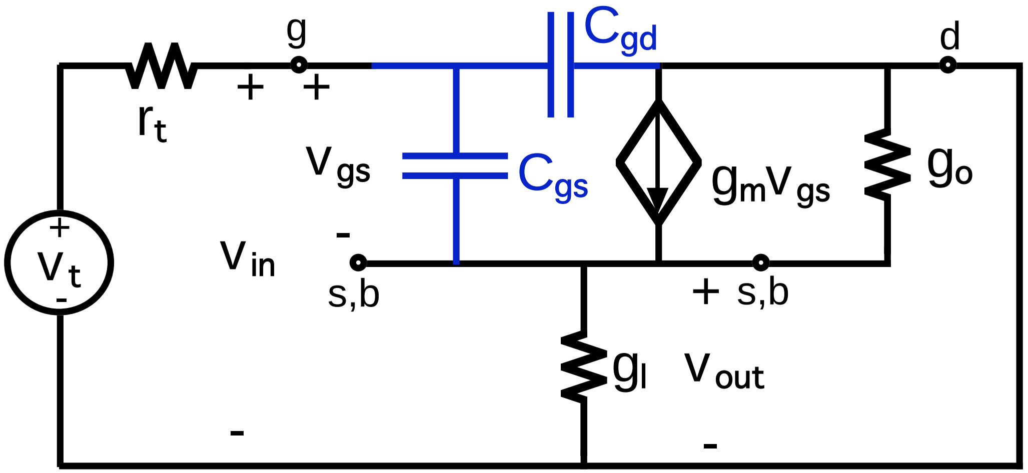


$$C_m \frac{(1-A_v)}{A_v} \approx C_m$$

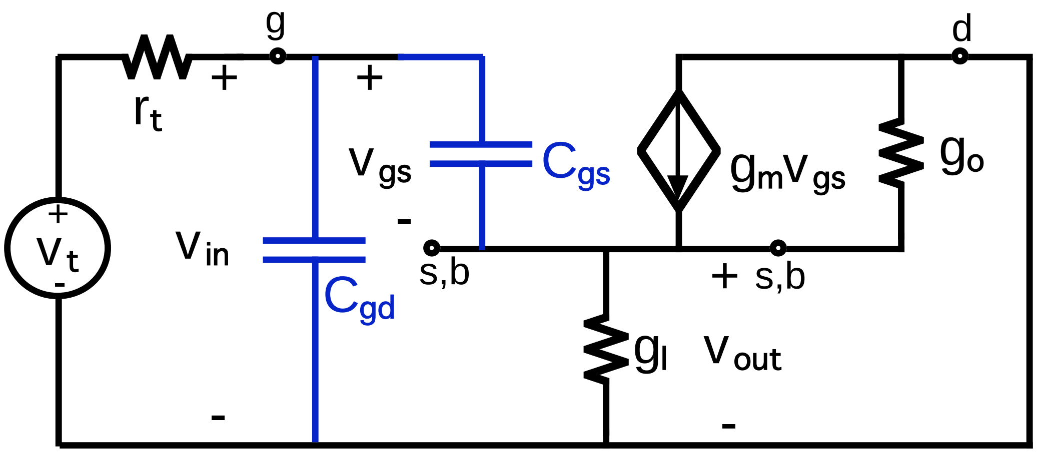
C_{out} looks like C_m

The Miller effect: Miller capacitors in other basic stages

Common drain or source follower



Repositioning C_{gd} makes the situation clearer:

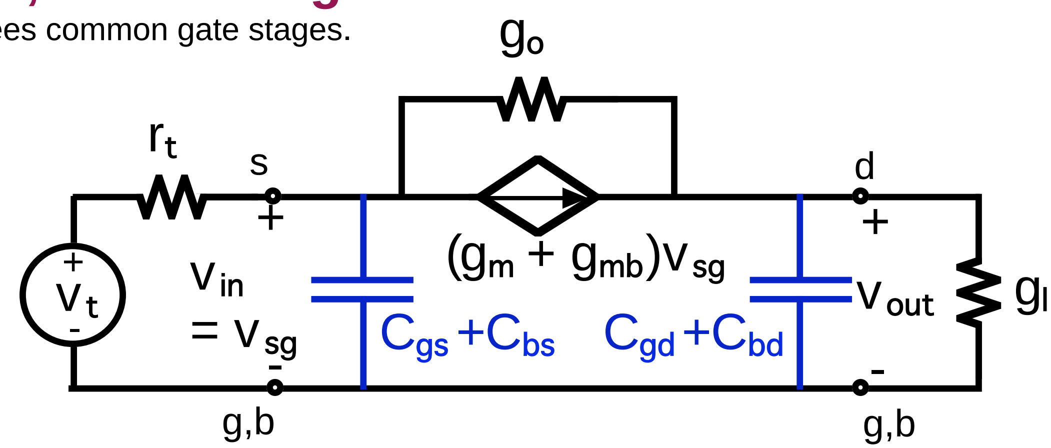


C_{gs} is in the Miller position, but the voltage gain is one so there is no Miller effect.

The Miller effect: Miller capacitors in other basic stages

Common gate, substrate grounded

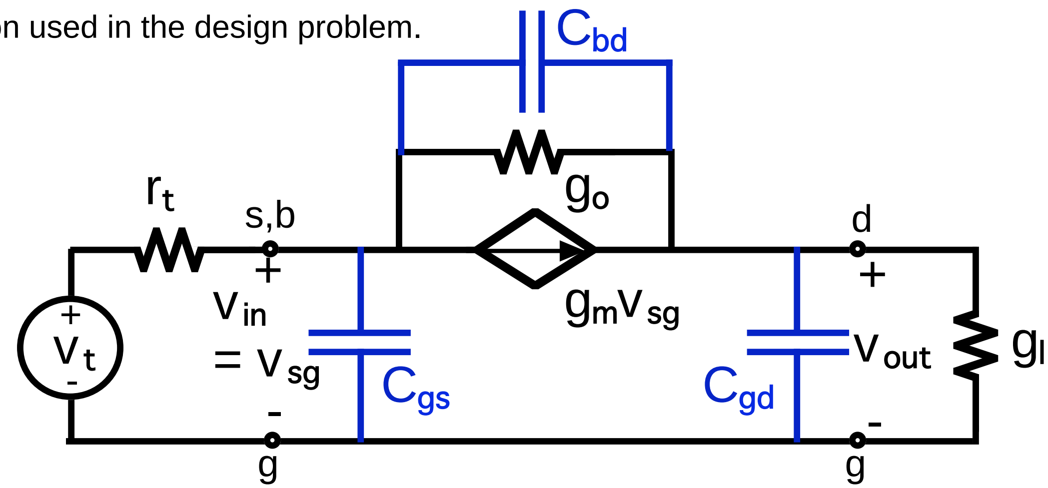
The way one often sees common gate stages.



No Miller effect, just as in common-base.

Common gate, substrate shorted to source

This is the connection used in the design problem.



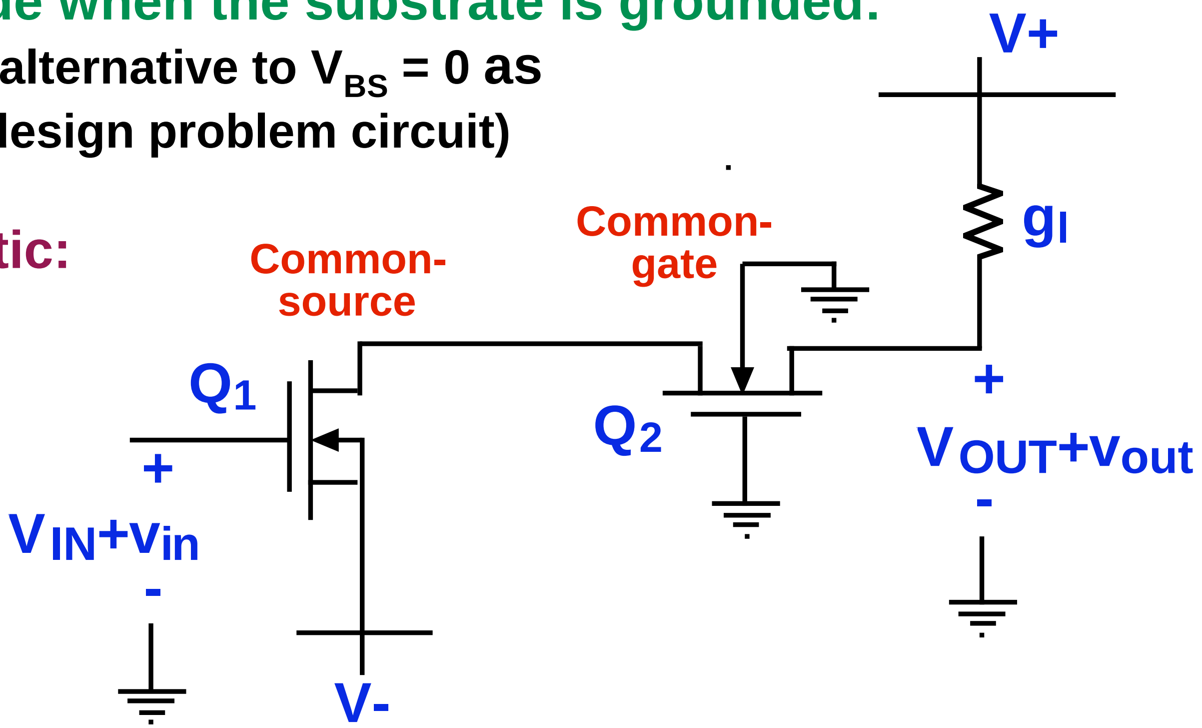
Now C_{bd} shows up in the Miller position.

- **But note that the gain is positive, so $(1-A_v)$ is negative and $C_{gs}||(1-A_v)C_{bd}$ is < C_{gs}, i.e. the Miller effect helps!**

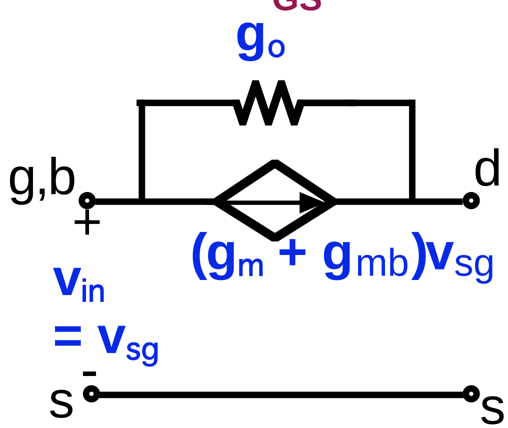
The cascode when the substrate is grounded:

$V_{BS} \neq 0$ (alternative to $V_{BS} = 0$ as in the design problem circuit)

Schematic:



Common-gate L.E.C. when $V_{GS} \neq 0$:

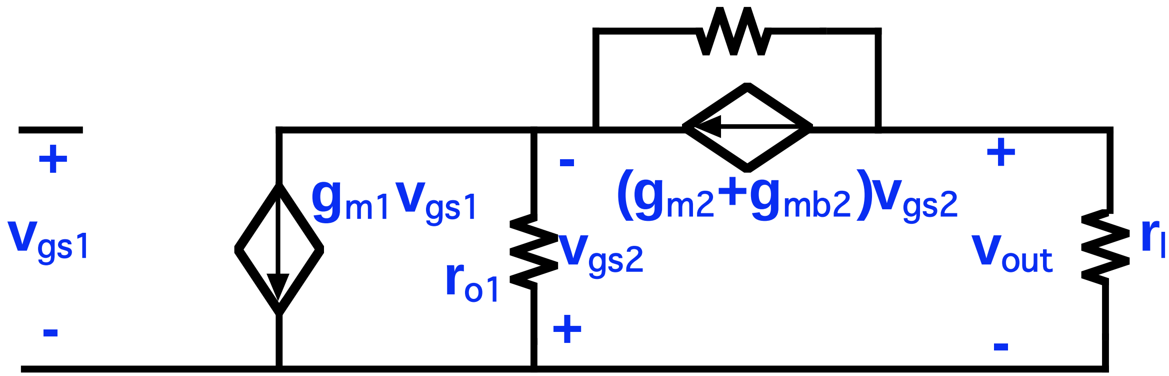


* The effective transconductance is increased by the substrate generator term.

The cascode when the substrate is grounded, cont:

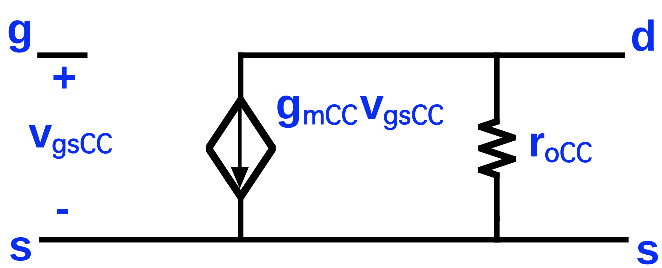
$V_{GS} \neq 0$

L.E.C.:



$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_l + \frac{g_{01}}{(g_{m2}+g_{mb2}+g_{02})}(g_l+g_{02})} \approx_o \frac{-g_{m1}}{g_l + g_{01}\frac{g_{02}}{(g_{m2}+g_{mb2})}}$$

The equivalent transistor, Q_{CC}:



$$g_{m,CC} = g_{m1} \qquad r_{o,CC} \approx r_{01}\frac{(g_{m2}+g_{mb2})}{g_{o2}}$$

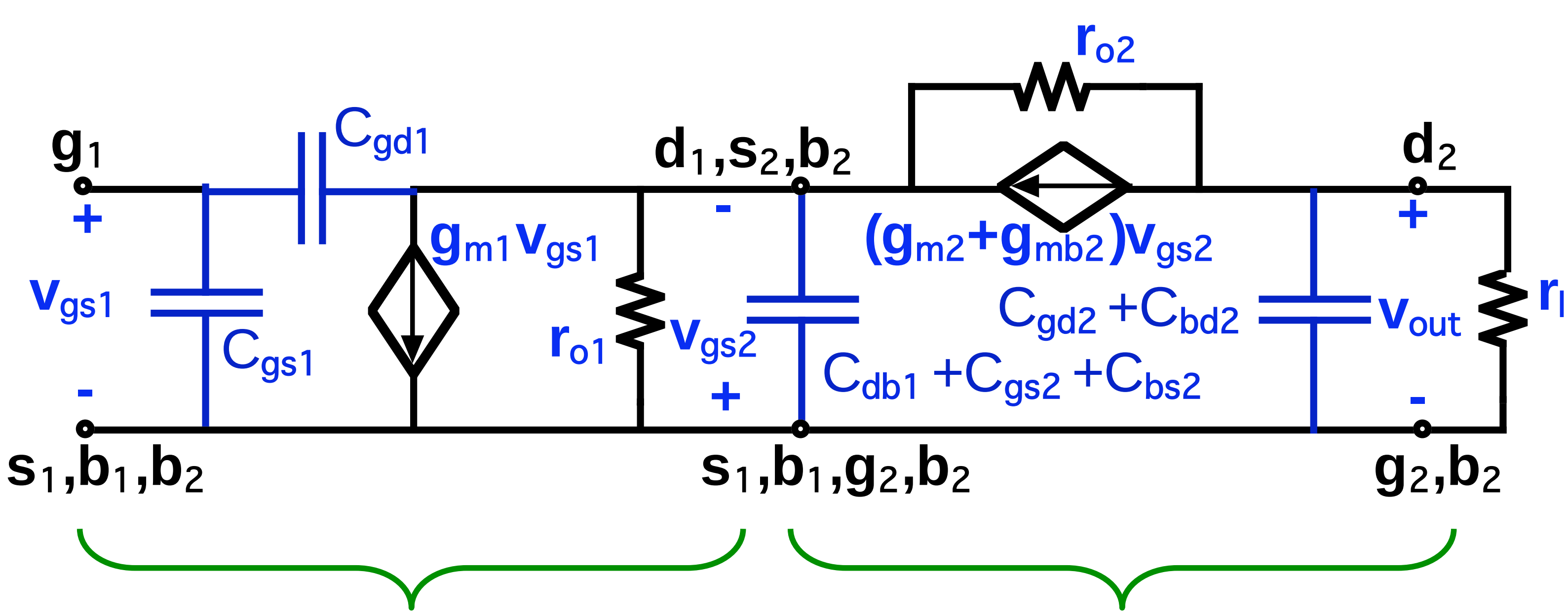
$$V_{A,CC} \approx V_{A1}\frac{(g_{m2}+g_{mb2})}{g_{o2}}$$

The output resistance is even higher!

The cascode when the substrate is grounded, cont:

High frequency issues:

L.E.C. of cascode: can't use equivalent transistor idea here because it didn't address the issue of the C's!



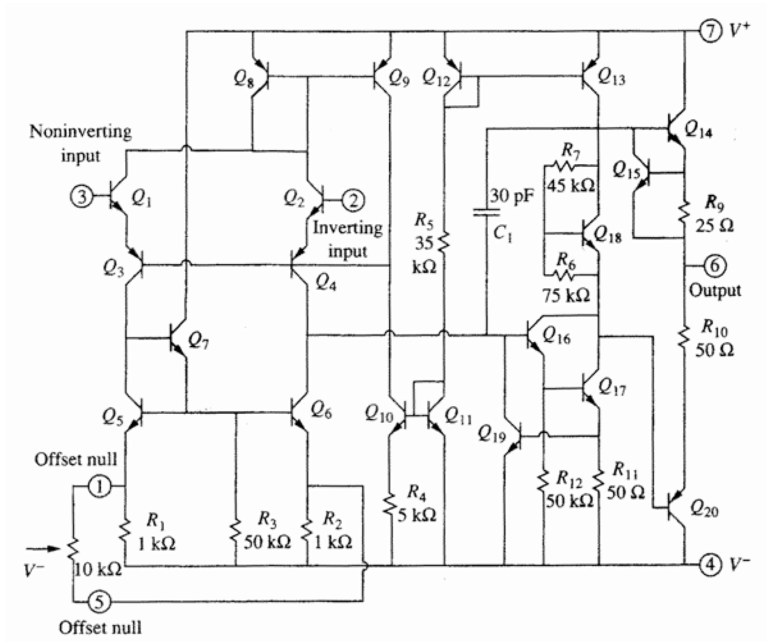
Voltage gain ≈ -1 so minimal Miller effect.

Voltage gain ≈ $g_m r_l$, without Miller effect.

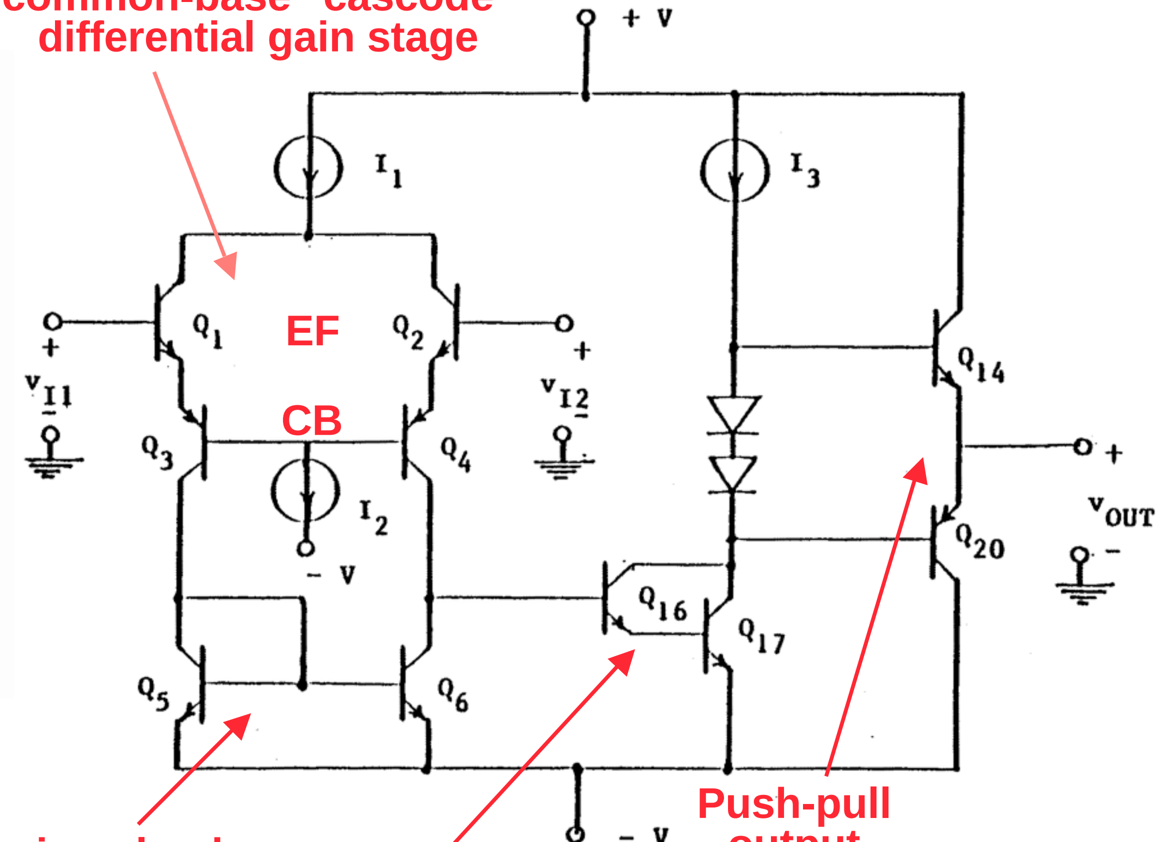
Common-source gain without the Miller effect penalty!

Multi-stage amplifier analysis and design: The μA741

Figuring the circuit out:



The full schematic

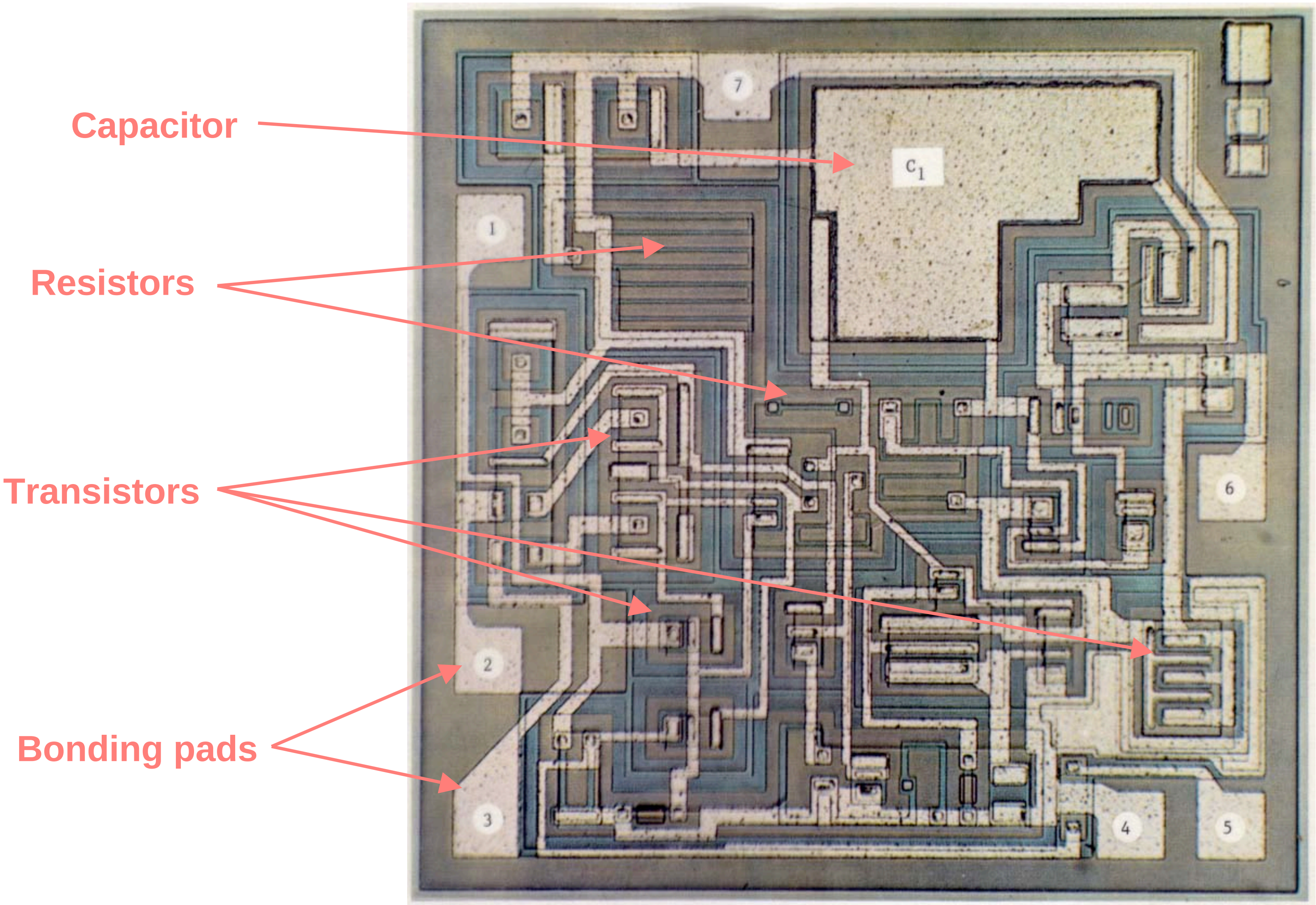


Simplified schematic

Another interesting discussion of the μA741:
http://en.wikipedia.org/wiki/Operational_amplifier

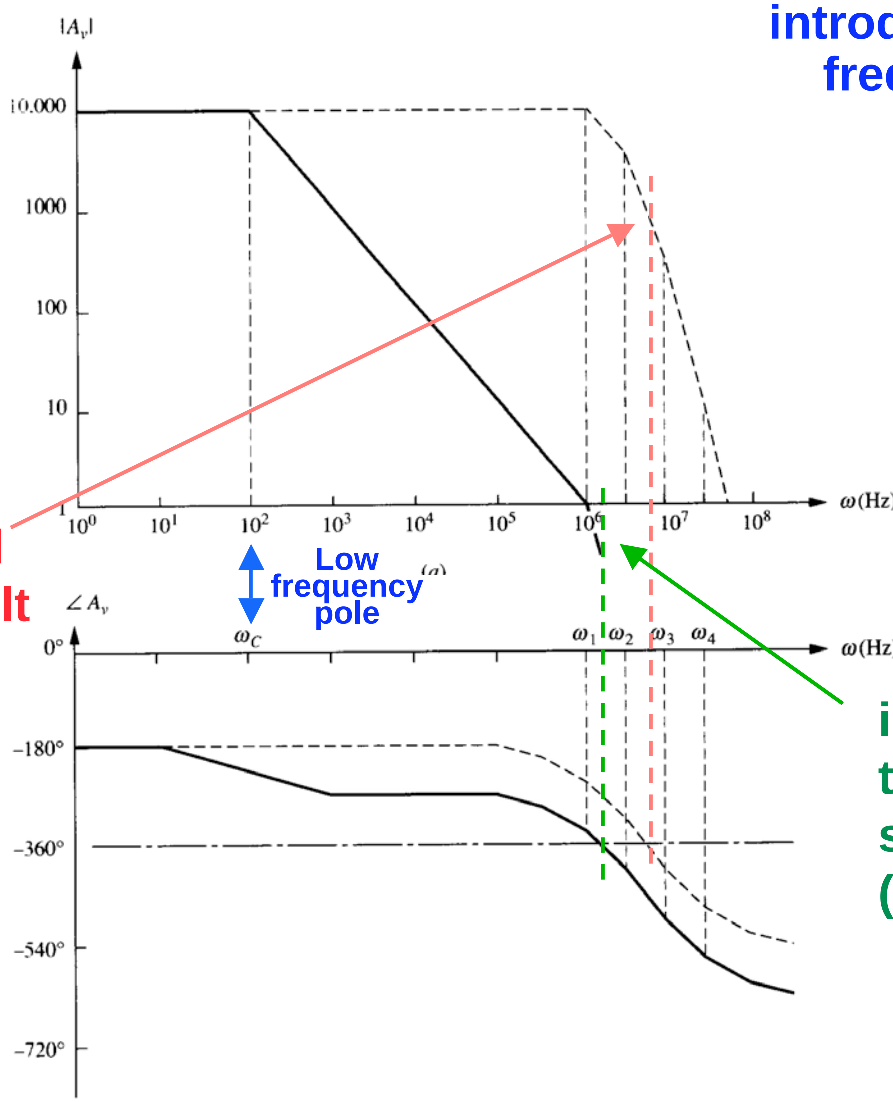
Multi-stage amplifier analysis and design: The µA741

The chip: a bipolar IC



Multi-stage amplifier analysis and design: The µA741

Why is there a capacitor in the circuit?: the added capacitor introduces a low frequency pole.



Without it the gain is still greater than 1 when the phase shift exceeds 180° (dashed curve**). This can result in positive feedback and instability.**

With it the gain is less than 1 by the time the phase shift exceeds 180° (solid curve**).**

Lecture 23 - Circuits at High Frequencies - Summary

Bounding mid-band - finding ω_{HI}, ω_{LO}

ω_{HI}: Find the resistance in parallel with each device capacitor assuming the such device capacitors are open circuits, calculate all the RC time constants, and add them. The inverse is a lower bound on ω_{HI}.

ω_{LO}: Find the resistance in parallel with each bias capacitor assuming the other such capacitors are short circuits, calculate all the 1/RC frequencies, and add them. This sum is an upper bound on ω_{LO}.

The Miller effect: why C_{gd} is so important

The concept: a capacitor shunting a gain stage looks larger by $(1 - A_v)$

Examples: (1) The Miller effect magnifies C_{gd} in common-source stages; (2) There is no significant Miller effect impact on common-gate stages or on source-followers; (3) The Miller effect is used in the µA741 to get the relatively large capacitor needed to stabilize it.

The Marvelous cascode

Concept and ω_{HI}: Current gain from a CS stage and voltage gain from a CG to circumvent the Miller effect.

Output resistance: significantly larger than CS alone.

The costs: The added device increases the voltage distance away from the rails and limits voltage swings