

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology*

6.012 Electronic Devices and Circuits

Final Exam

Monday, May 19, 2008

9:00 am to 12 noon

Closed Book: Formula sheet provided; 3 sheets of notes permitted

Notes:

1. Unless otherwise indicated, you should assume room temperature and that kT/q is 0.025 V. You should also approximate $[(kT/q) \ln 10]$ as 0.06 V.
2. Closed book; three sheets (6 pages) of notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all twelve (12) pages of this exam booklet and the eight (8) page formula sheet, and make certain that you write your name at the top of this page in the space provided.
7. An effort has been made to make the various parts of these problems independent of each other so if you have difficulty with one item go on, and come back later.
8. You may see your graded final exam beginning June 2, 2008.

6.012 Staff Use Only	PROBLEM 1	_____	(out of a possible 25)
	PROBLEM 2	_____	(out of a possible 25)
	PROBLEM 3	_____	(out of a possible 25)
	PROBLEM 4	_____	(out of a possible 25)
	TOTAL	<div style="border: 1px solid black; width: 100px; height: 40px; display: inline-block;"></div>	

Problem 1 - (25 points)

a) [4 pts] A local company has succeeded in making n-type gallium nitride (GaN) in which the hole-electron recombination process in the quasi-neutral regions is very efficient at producing blue light. They want your help designing p-n diodes to take advantage of this material to produce efficient blue light emitting diodes.

i) What type of diodes do you recommend they make, p⁺-n, p-n, or p-n⁺, and why?

p⁺-n ($N_{Ap} \gg N_{Dn}$) p-n ($N_{Ap} \approx N_{Dn}$) p-n⁺ ($N_{Ap} \ll N_{Dn}$)
because

ii) To optimize the width of n-region, w_n , to get a large fraction of the possible emission without making the layers excessively thick, how large would you recommend they make w_n (compared to the minority carrier diffusion length, L_h), and why?

$w_n = 3 \text{ to } 4 L_h$ $w_n \approx L_h$ $w_n = L_h/3$, or less
because

b) [6 pts] So those of you who studied BJTs aren't disappointed, and so those of you who didn't should still be able to get some points, here are the only BJT questions on the final. Ten (10) word answers, or less.

i) What is the physical origin of the Early effect in a BJT, and how is it minimized in a well designed device?

Physical origin of the Early effect:

Design rule to minimize it:

ii) Why is an npn BJT preferred over a pnp BJT for high current gain and high speed? [Hint: same reason n-channel is preferred over p-channel MOSFET]

iii) What is the meaning of f_T (or ω_T) of a BJT (or any transistor, for that matter), and how does it depend on the base width, w_B ?

Meaning:

Dependence on w_B :

Problem 1 continues on the next page

Problem 1 continued

- c) [6 pts] Rank order the following three MOSFET linear amplifier stages in order of increasing output resistance, and give an approximate value for the output resistance if the transistors in each stage are biased in saturation with $V_{BS} = 0$, and so that $g_m = 0.2 \text{ mS}$, and $g_o = g_t = 10 \mu\text{S}$: common-source, common-gate, source follower (common drain). Assume the biasing is done with ideal current sources.

i) Lowest output resistance: Stage _____

Approx. Value: _____ Ohms

ii) Intermediate output resistance: Stage _____

Approx. Value: _____ Ohms

iii) Highest output resistance: Stage _____

Approx. Value: _____ Ohms

- d) [6 pts] The source, drain and substrate of a MOSFET are shorted together and the small signal capacitance of the gate relative to this composite terminal, C_g , is measured. It is observed that C_g is constant and equal to WLC_{ox}^* when V_{GS} is less than -0.1 V or greater than 0.3 V , but that when V_{GS} is between -0.1 V and 0.3 V C_g is smaller, with the minimum value occurring near -0.1 V .

i) What are the flat-band voltage, V_{FB} , and threshold voltage, V_T , of this transistor?

$V_{FB} = \underline{\hspace{2cm}}$ Volts

$V_T = \underline{\hspace{2cm}}$ Volts

ii) What type of MOSFET is this, n-channel or p-channel, and why?

n-channel p-channel

because

Problem 1 continues on the next page

Problem 1 continued

iii) How does C_{gs} in the linear equivalent circuit model of a MOSFET operating in the sub-threshold region compare to WLC_{ox}^* ?

Greater than Less than Similar to
because

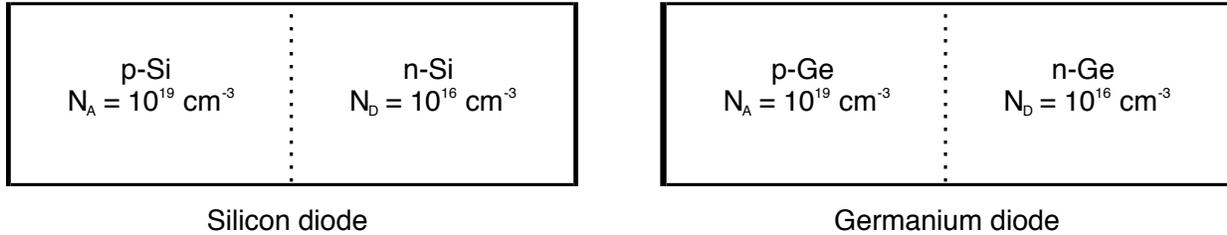
e) [3 pts] An isolated n-type silicon sample with $N_D = 10^{17} \text{ cm}^{-3}$, minority carrier lifetime, τ_{minor} , equal to 10^{-5} s , and perfectly reflecting boundaries (i.e., no surface recombination) has been illuminated for a long time with light generating 10^{20} hole-electron pairs/ $\text{cm}^3\text{-s}$ uniformly throughout its bulk. At $t = 0$ the light is extinguished. What is the excess minority carrier density in this sample as a function of time for $t \geq 0$?

$$p'(t \geq 0) = \underline{\hspace{10cm}} \text{ cm}^{-3}$$

End of Problem 1

Problem 2 (25 points)

Consider the two asymmetrically doped p-n junction diodes shown below that have identical uniform doping profiles, but are made of different semiconductors: one is made of silicon (Si), and the other is made of germanium (Ge). The room temperature intrinsic carrier concentration for Ge, n_{i-Ge} , is $\sqrt{5} \times 10^{13} \text{ cm}^{-3}$ and the dielectric constant, ϵ_{Ge} , is $1.6 \times 10^{-12} \text{ F/cm}$; for Si, $n_{i-Si} = 10^{10} \text{ cm}^{-3}$ and $\epsilon_{Si} = 10^{-12} \text{ F/cm}$.



- a) [4 pts] Calculate the thermal equilibrium minority hole concentration, p_o , in the quasi-neutral region on the n-side of each of these diodes.

$$p_{no,Si} = \underline{\hspace{2cm}} \text{ cm}^{-3}$$

$$p_{no,Ge} = \underline{\hspace{2cm}} \text{ cm}^{-3}$$

- b) [4 pts] Calculate the built-in potential, ϕ_b , for the Si and Ge diodes. As needed, you may use $\log 5 = 0.7$, and $(kT/q) \ln 10 = 60 \text{ mV}$.

$$\phi_{b,Si} = \underline{\hspace{2cm}} \text{ Volts}$$

$$\phi_{b,Ge} = \underline{\hspace{2cm}} \text{ Volts}$$

- c) [4 pts] Calculate the ratio of the depletion width on the n-side of the Ge diode to that of the Si diode in thermal equilibrium, i.e. x_{n-Ge}/x_{n-Si} .

$$x_{n-Ge}/x_{n-Si} = \underline{\hspace{2cm}}$$

Problem 2 continues on the next page

Problem 2 continued

- c) [4 pts] Calculate the ratio of the junction depletion capacitances of the two diodes in thermal equilibrium.

$$C_{\text{dp-Ge}}/C_{\text{dp-Si}} = \underline{\hspace{2cm}}$$

NOTE: For the rest of this problem assume that the diffusion coefficient for electrons is the same in both materials, and the same for holes. Also, assume that the lengths of the corresponding quasi-neutral regions are the same and that carrier recombination only takes place at the contacts (i.e., that the minority carrier lifetime in the bulk regions is infinite).

- d) [5 pts] The two diodes are forward biased so that their currents are the same. What is the ratio of the excess minority carrier density at the edge of the depletion region on the n-side of the Ge diode to that of the Si diode?

$$p'(x_{n+\text{Ge}})/p'(x_{n+\text{Si}}) = \underline{\hspace{2cm}}$$

- e) [4 pts] Calculate the difference of the forward voltage, V_{AB} , that is applied to the two diodes when the current through them is the same, as in Part d.

$$V_{\text{AB-Ge}} - V_{\text{AB-Si}} = \underline{\hspace{2cm}} \text{ Volts}$$

End of Problem 2

Problem 3 - (25 points)

This problem studies the performance of state-of-the-art MOSFET transistors in digital electronics. In modern CMOS technology, the physical parameters of transistors with minimum dimensions are as follow:

Gate oxide thickness, t_{ox} : 1.0 nm (10^{-7} cm)

Oxide dielectric constant, ϵ_{ox} : 3.5×10^{-13} F/cm

Gate length, L_{min} : 35 nm

Gate width, W_{min} : 135 nm

Supply voltage, V_{DD} : 1.0 V

Threshold voltage: $V_{T,n} = -V_{T,p} = 0.4$ V

Electron mobility, μ_e : 500 cm²/Vs

Hole mobility, μ_h : 200 cm²/Vs

Sub-threshold current when $|V_{GS}| = 0$: 15 nA (n-channel and p-channel)

Early effect: $\lambda_n = \lambda_p = 10^{-3}$ V⁻¹

Alpha factor, α : ≈ 1

- a) [4 pts] Calculate the drain current in saturation, $I_{D,sat}$ of a minimum size n-MOS transistor in this technology when $V_{GS} = V_{DD} = 1.0$ V. Use the general expression we derived using the gradual channel approximation model in strong inversion and assume $\alpha = 1$ and that the low-field mobility model is valid.

$$I_{D,sat}(V_{GS} = 1.0 \text{ V}) = \underline{\hspace{2cm}} \text{ A}$$

- b) [3 pts] Calculate the value of the output resistance, r_o , in the small signal linear equivalent circuit of the n-MOS transistor in saturation with $V_{GS} = 1.0$ V.

$$r_o = \underline{\hspace{2cm}} \text{ Ohms}$$

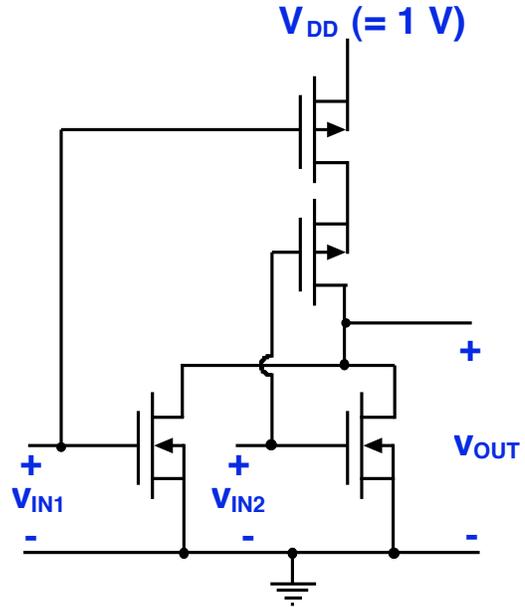
Problem 3 continues on the next page

Problem 3 continued

The CMOS NOR gate shown to the right is fabricated using the new technology.

- c) [2 pts] Fill in the truth table below for this gate. Ignore the sub-threshold drain current when the FETs are off.

V_{IN1}	V_{IN2}	V_{OUT}
0 V	0 V	_____ V
0 V	1 V	_____ V
1 V	0 V	_____ V
1 V	1 V	_____ V



- d) [3 pts] In a simple CMOS inverter both transistors are minimum gate length devices, $L_n = L_p = L_{min}$, and the widths are scaled so that $K_n = K_p$, with the narrowest gate being made W_{min} . What should W_n and W_p be in a simple inverter made with this process (i.e., as described at the start of this problem statement)? Note: The multiples do not have to be integer.

$$W_{n,Inverter} = \text{_____} W_{min}$$

$$W_{p,Inverter} = \text{_____} W_{min}$$

- e) [4 pts] To size the FETs in a NOR gate for minimum switching time, one must recognize that two p-FETs in series with the same voltage on their gates, as in a NOR gate when both inputs are low, function like one FET with $L = 2L$ (and $W = W_p$). What is the optimum size of the p-channel MOSFETs in a NOR gate fabricated with the process described earlier, and what is the load seen at the input of such a NOR gate, compared to an inverter? Note: The multiples can be non-integer. (The n-channel FET should be kept the same size as in a simple inverter because turning either n-FET “on” pulls the output low.)

$$L_{p,NOR} = \text{_____} L_{min}$$

$$W_{p,NOR} = \text{_____} W_{min}$$

$$C_{IN,NOR} = \text{_____} C_{IN,Inverter}$$

Problem 3 continues on the next page

Problem 3 continued

- f) [3 pts] What is the static power dissipation in a microprocessor containing 2×10^9 equivalent NOR gates like the one shown on the previous page? Assume that for half of the gates the output is low and for half of the gates it is high. Be careful.

$$P_{\text{Static}} = \underline{\hspace{2cm}} \text{ Watts}$$

- g) [6 pts] When the n-channel transistor in Part a) was fabricated, the actual saturation current with $V_{\text{GS}} = V_{\text{DS}} = 1$ Volt was measured to be only $250 \mu\text{A}$. To try to figure out what is wrong, do the following three calculations, and then give an opinion:

- i) Calculate the average electric field in the channel with $V_{\text{GS}} = V_{\text{DS}} = 1$ Volt.

$$E_{\text{ave}} = \underline{\hspace{2cm}} \text{ V/cm}$$

- ii) Calculate what the average electron velocity in the channel with $V_{\text{GS}} = V_{\text{DS}} = 1$ Volt and a drain current of $250 \mu\text{A}$ is. Assume a uniform inversion charge distribution along the channel.

$$s_{\text{ch,ave}} (I_{\text{D}} = 250 \mu\text{A}) = \underline{\hspace{2cm}} \text{ cm/s}$$

Calculate the what average electron velocity in the channel would be with $V_{\text{GS}} = V_{\text{DS}} = 1$ Volt and the drain current you calculated in Part a. Approximate the inversion charge distribution along the channel as being uniform. If you couldn't do Part a use a drain current of 1 mA (this is not the right answer for Part a).

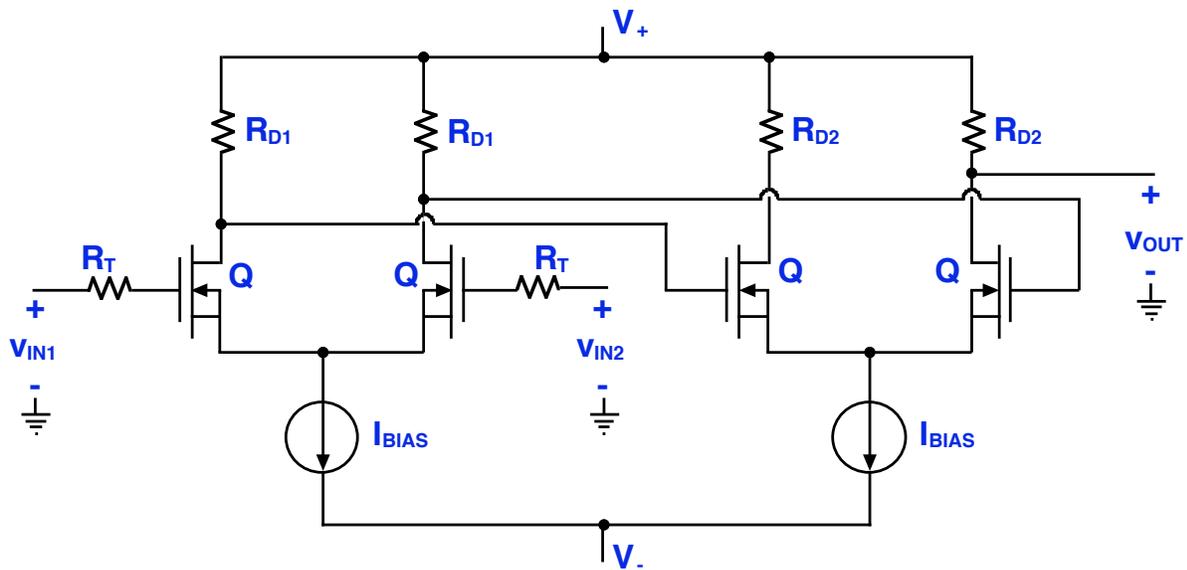
$$s_{\text{ch,ave}} (I_{\text{D}} = \text{answer in Part a}) = \underline{\hspace{2cm}} \text{ cm/s}$$

- iii) Why (in 25 words or less) do you think the measured drain current is so much lower than you predicted in Part a?

End of Problem 3

Problem 4 - (25 points)

The transistors in the two-stage differential amplifier shown below are all identical with $V_T = 0.4$ V, $C_{gs} = 3$ pF, $C_{gd} = 1$ pF, and $\lambda = 0$ V⁻¹, and all are biased so that $g_m = 6$ mA/V. The values of the resistances are: $R_{D1} = R_{D2} = 5$ k Ω , and $R_T = 50$ k Ω . The current sources can be considered to be ideal.



- a) [4 pts] Calculate the mid-band differential mode voltage gain, A_{vd} , of the amplifier, where A_{vd} is defined by $v_{out} = A_{vd}[v_{in1} - v_{in2}] + A_{vc}[(v_{in1} + v_{in2})/2]$?

$$A_{vd} = \underline{\hspace{2cm}}$$

- b) [3 pts] What is the mid-band common mode voltage gain, A_{vc} , of this amplifier, where A_{vc} is defined by $v_{out} = A_{vd}[v_{in1} - v_{in2}] + A_{vc}[(v_{in1} + v_{in2})/2]$?

$$A_{vc} = \underline{\hspace{2cm}}$$

Problem 4 continues on the next page

Problem 4 continued

- c) [4 pts] If $V_+ = 1.5 \text{ V}$, $V_- = -1.5 \text{ V}$, and $I_{\text{BIAS}} = 0.2 \text{ mA}$, and if the transistors are all biased with $(V_{\text{GS}} - V_{\text{T}}) = 0.2 \text{ V}$, what is the maximum common-mode input voltage for this amplifier?

$$V_{\text{IC,max}} = \text{_____ Volts}$$

- d) [3 pts] Calculate the quiescent power dissipation in this amplifier, P_{Q} , under the bias conditions specified in Part c?

$$P_{\text{Q}} = \text{_____ Watts}$$

- e) [3 pts] What value of R_{D2} would make the quiescent output voltage, V_{OUT} , zero? (Note: Do not change R_{D2} to this value in the remaining parts of this question; it should stay $5 \text{ k}\Omega$.)

$$R_{\text{D2}} = \text{_____ Ohms}$$

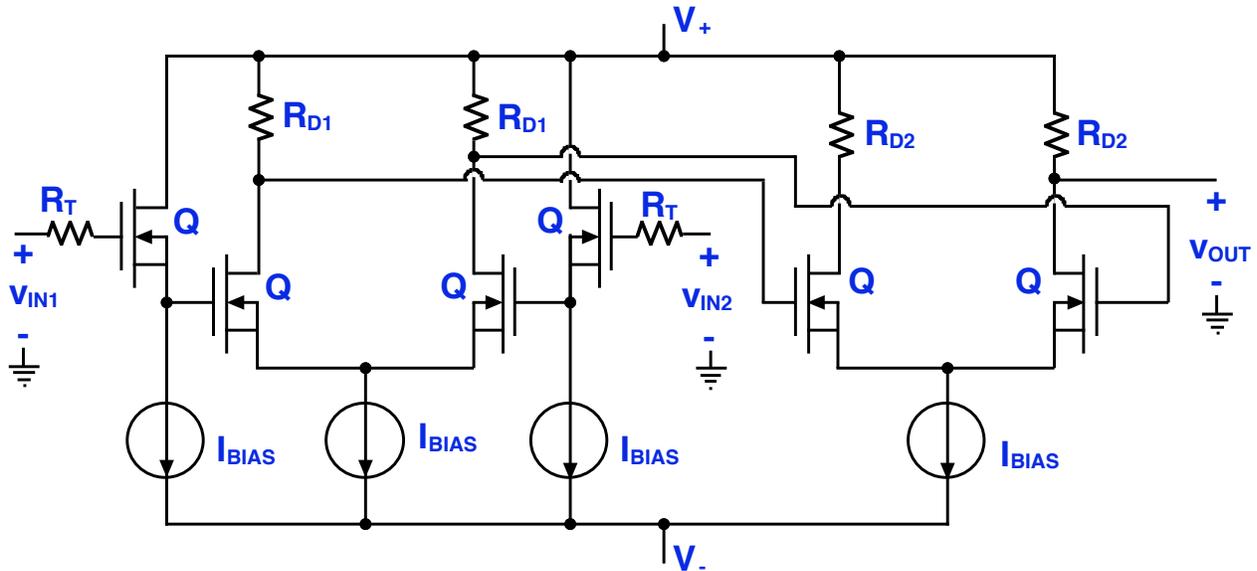
- f) [4 pts] Calculate the bandwidth, ω_{HI} , of the amplifier in differential mode. Assume C_{db} is negligible, and use the Miller effect to combine C_{gs} and C_{gd} at the input to each stage, before you calculate the open circuit time constants to estimate ω_{HI} .

$$\omega_{\text{HI}} = \text{_____ } \text{s}^{-1}$$

Problem 4 continues on the next page

Problem 4 continued

- g) [4 pts] To increase the bandwidth of the circuit, we add a third amplifier stage (a preamplifier) to each input as shown in the figure below. The transconductance of the two new transistors is also $g_m = 6 \text{ mS}$.



In the space below, explain in 25 words or less why the bandwidth is increased by this change. You can assume that the open circuit time constants associated with the intrinsic capacitances of the preamplifier transistors do not contribute to ω_{HI} .

End of Problem 4; end of Final Exam. Have a great summer.

MIT OpenCourseWare
<http://ocw.mit.edu>

6.012 Microelectronic Devices and Circuits
Fall 2009

For information about citing these materials or our Terms of Use, visit: <http://ocw.mit.edu/terms>.