

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology*

6.012 Electronic Devices and Circuits

Exam No. 2

Wednesday, April 19, 2006

7:30 to 9:30 pm

Notes:

1. Unless otherwise indicated, you should assume room temperature and that kT/q is 0.025 V. You should also approximate $[(kT/q) \ln 10]$ as 0.06 V.
2. Closed book; two sheets (4 pages) of notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all ten (10) pages of this exam booklet and the four (4) page formula sheet, and make certain that you write your name at the top of this page in the space provided.
7. An effort has been made to make the various parts of these problems independent of each other so if you have difficulty with one item go on, and come back later.

6.012 Staff Use Only	PROBLEM 1	_____	(out of a possible 36)
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	PROBLEM 2	_____	(out of a possible 32)
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	PROBLEM 3	_____	(out of a possible 32)
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	TOTAL		
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Problem 1 - (36 points)

Part (a) concerns the large signal and linear equivalent circuit models for MOSFETs and Part (b) concerns these same models for BJTs. Part (c) concerns CMOS inverters. There are 18 short questions, each worth 2 points, so move along spritely!

a) [12 pts] Consider two well-designed n-channel MOSFETs, M_A and M_B , that are identical in structure and dimension except that the gate length, L , of M_A is twice that of M_B . How do the following parameters compare? Explain your answers.

i) The K factor in the gradual channel approximation model for the drain current:

A greater than B A less than B A similar to B
because

ii) The threshold voltage, V_T :

A greater than B A less than B A similar to B
because

iii) The quiescent gate-to-source voltage, V_{GS} , at the bias point $I_D = 0.5 \text{ mA}$, $V_{DS} = 5 \text{ V}$:

A greater than B A less than B A similar to B
because

iv) The incremental model output conductance, g_o , at the bias $I_D = 0.5 \text{ mA}$, $V_{DS} = 5 \text{ V}$:

A greater than B A less than B A similar to B
because

v) The incremental model gate-to-source capacitance, C_{gs} , at the bias $I_D = 0.5 \text{ mA}$, $V_{DS} = 5 \text{ V}$:

A greater than B A less than B A similar to B
because

vi) The incremental model gate-to-drain capacitance, C_{gd} , at the bias $I_D = 0.5 \text{ mA}$, $V_{DS} = 5 \text{ V}$:

A greater than B A less than B A similar to B
because

Problem 1 continues on the next page

Problem 1 continued

b) [12 pts] Consider two well-designed npn bipolar junction transistors, Q_A and Q_B , which both have a large current gain, β , and large Early voltage, V_A . They are identical in structure except that the base of Q_A is doped twice as heavily as the base of Q_B . How do the following parameters or values compare? Explain your answers.

i) The base-emitter diode saturation current in the Ebers-Moll model, I_{ES} :

A greater than B A less than B A similar to B
because

ii) The base-collector diode saturation current in the Ebers-Moll model, I_{CS} :

A greater than B A less than B A similar to B
because

iii) Forward common-emitter current gain, β_F :

A greater than B A less than B A similar to B
because

iv) Linear equivalent circuit transconductance, g_{mv} , for the bias $I_C = 1$ mA, $V_{CE} = 5$ V:

A greater than B A less than B A similar to B
because

v) Linear equivalent circuit output conductance, g_o , for the bias $I_C = 1$ mA, $V_{CE} = 5$ V:

A greater than B A less than B A similar to B
because

vi) Linear equivalent circuit collector-base capacitance, C_{μ} , for the bias point $I_C = 1$ mA and $V_{CE} = 5$ V:

A greater than B A less than B A similar to B
because

Problem 1 continues on the next page

Problem 1 continued

c) [12 pts] The gates on a CMOS logic chip were laid out by a designer who had not taken 6.012 and they have $W_p = W_{\min}$ and $W_n = 2 W_{\min}$ instead of $W_n = W_{\min}$ and $W_p = 2 W_{\min}$. What was the impact of this error on the following inverter performance metrics relative to the usual case of an inverter with $W_n = W_{\min}$ and $W_p = 2 W_{\min}$? Explain your answers.

i) Inverter input capacitance, C_L :

Increased Decreased Essentially unchanged
because

ii) The output node charging current after the input has switched from HI to LO:

Increased Decreased Essentially unchanged
because

iii) The output node discharge current after the input has switched from LO to HI:

Increased Decreased Essentially unchanged
because

iv) Static power dissipation:

Increased Decreased Essentially unchanged
because

v) The logic HI voltage:

Increased Decreased Essentially unchanged
because

vi) The noise margins:

Both increased Both decreased
 One increased, one decreased Both essentially unchanged
because

End of Problem 1

Problem 2 (32 points)

You are given an silicon npn bipolar transistor with the following parameter values and Gummel plot:

$$W_E = 0.25 \mu\text{m}, \quad W_B = 0.5 \mu\text{m} \quad W_C = 1.0 \mu\text{m}$$

$$\text{Active device cross-sectional areas: } A_E = A_C = 10^4 \text{ cm}^2$$

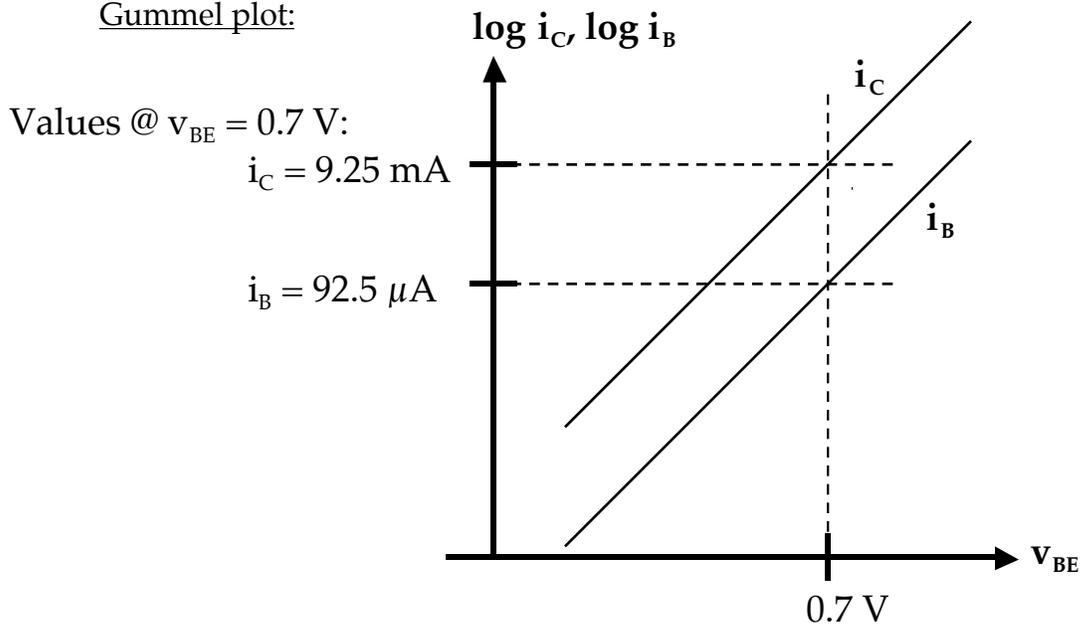
$$D_h = 10 \text{ cm}^2/\text{s}, \quad D_e = 20 \text{ cm}^2/\text{s}$$

Minority carrier lifetime, $\tau_{\text{min}} = \infty$ (recombination only at contacts)

$$\text{Collector doping, } N_{DC} = 5 \times 10^{16} \text{ cm}^{-3}$$

$$V_A = 100 \text{ V}$$

Gummel plot:



a) [3 pts] What is the forward current gain, β_F , in this transistor?

$$\beta_F = \underline{\hspace{2cm}}$$

b) [2 pts] What is the base defect, δ_B , in this transistor?

$$\delta_B = \underline{\hspace{2cm}}$$

Problem 2 continues on the next page

Problem 2 continued

- c) [6 pts] Calculate the ratio, r , defined as $r = (w_{E,\text{eff}} \cdot N_{DE}) / (w_{B,\text{eff}} \cdot N_{AB})$.

$$r = \underline{\hspace{2cm}}$$

- d) [6 pts] Calculate the net acceptor concentration in the base, N_{AB} . (Hint: Do not use your answer in Part c.)

$$N_{AB} = \underline{\hspace{2cm}} \text{ cm}^{-3}$$

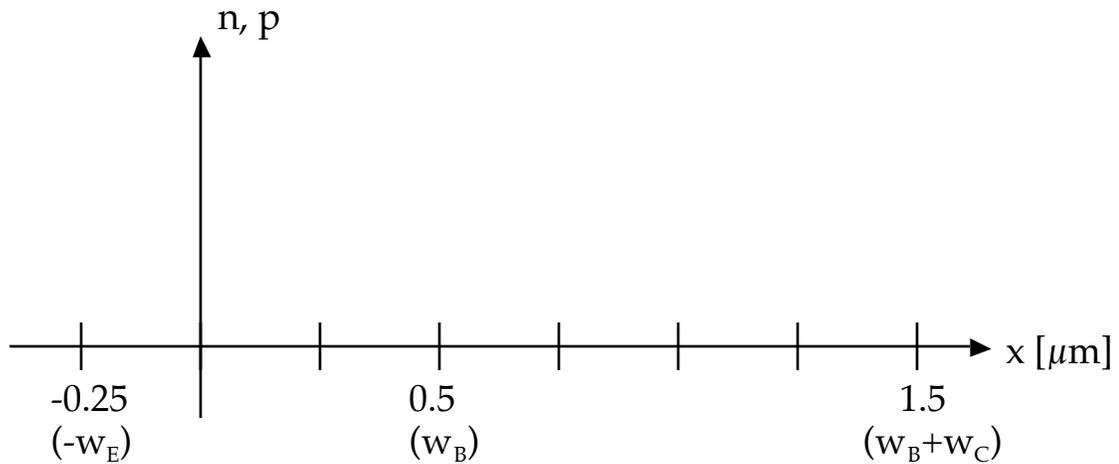
- e) [5 pts] Calculate the net donor concentration in the emitter, N_{DE} .

$$N_{DE} = \underline{\hspace{2cm}} \text{ cm}^{-3}$$

- f) [5 pts] On the axes provided at the top of the next page, draw the total minority carrier profiles for the bias condition $V_{BE} = 0.7 \text{ V}$, $V_{BC} = -1 \text{ V}$. Label the numerical values of the minority carrier concentrations at the edges of the depletion regions at $x = 0$ and $x = w_B$, and at the contacts. (Note: Neglect the depletion region widths relative to the emitter, base, and collector widths.)

Problem 2 continues on the next page

Problem 2 continued



- g) [5 pts] Consider the total number of excess minority carriers in the base of this transistor, $Q_{B,diff}$ under each of the following two bias conditions,

Bias A: $V_{BE} = 0.7 \text{ V}$ $V_{BC} = -1 \text{ V}$

Bias B: $V_{BE} = 0.7 \text{ V}$ $V_{BC} = 0.7 \text{ V}$

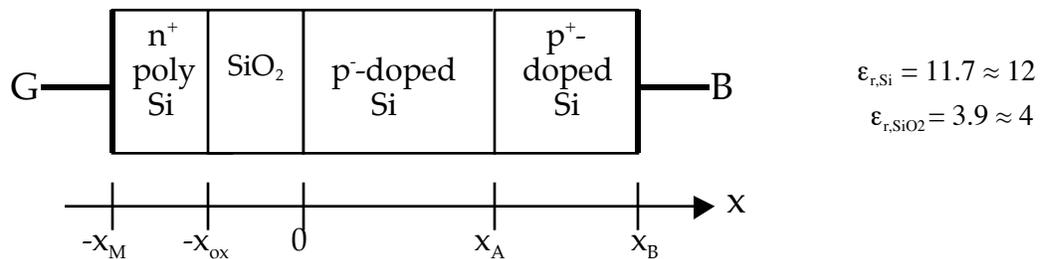
What is the ratio of the $Q_{B,diff}$'s under the two bias conditions? (Suggestion: Try sketching $n'(x)$ for $0 < x < w_B$ for each of these biases.)

$$Q_{B,diff}(\text{Bias A}) / Q_{B,diff}(\text{Bias B}) = \underline{\hspace{2cm}}$$

End of Problem 2

Problem 3 - (32 points)

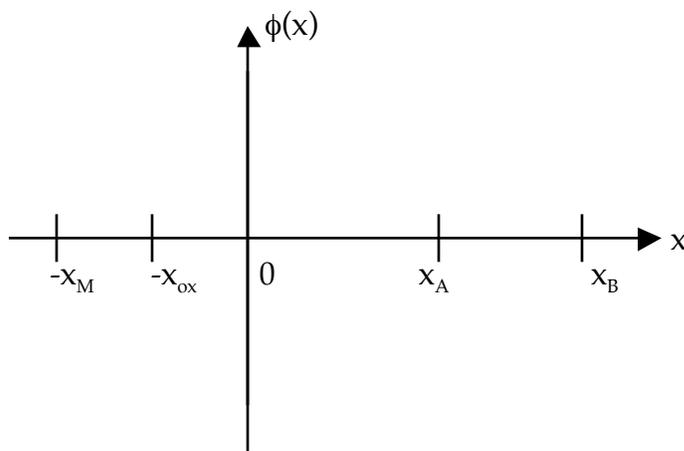
You are given a silicon MOS system as shown below. The region from $x = 0$ to x_A is very lightly doped p-type with $N_A = 10^{15} \text{ cm}^{-3}$, while the region beyond is heavily doped p-type. The doping levels in the n^+ poly gate and in the p^+ region are very high and not specified, but you are given that $\phi_{n^+} = 0.54 \text{ V}$ and $\phi_{p^+} = -0.54 \text{ V}$. The electrostatic potential of the contact and lead metal, $\phi_{m'}$ is 0.2 V . Any depletion regions in the n^+ and p^+ regions can be assumed to be of infinitesimal width, i.e. modeled as $Q'_n \delta(-x_{ox})$ and $Q'_p \delta(x_A)$, respectively. Also, $x_{ox} = 5 \text{ nm}$ and $x_A = 10 \text{ nm}$.



- a) [4 pts] What is the value of the flatband voltage, V_{FB} , for this MOS structure?

Flatband Voltage, $V_{FB} = \underline{\hspace{2cm}}$ Volts

- b) [5 pts] On the axes provided below, sketch carefully the electrostatic potential, $\phi(x)$, from G to B for $V_{GB} = 0 \text{ V}$. Assume that the lightly doped p-region is fully depleted. On your sketch indicate the potential difference between the bulks of the n^+ and p^+ regions.



Problem 3 continues on the next page

Problem 3 continued

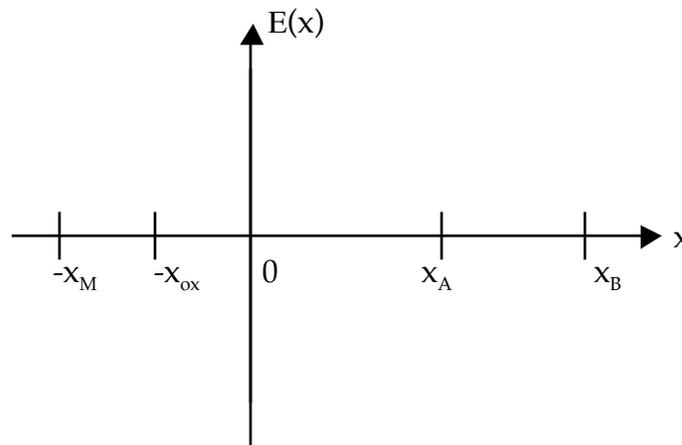
- c) [4 pts] To evaluate the assumption made in Part (b) that the lightly doped p-region is depleted, calculate the potential difference between $x = 0$ and $x = x_A$ that would just deplete this region. Explain why the assumption in Part (b) is, or isn't, justified.

Potential drop to just deplete the p-region: $\Delta\phi = \underline{\hspace{2cm}}$ V

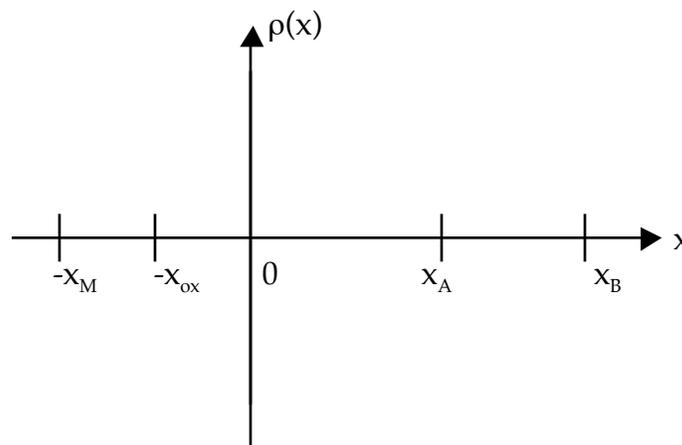
The assumption is is not justified because

- d) [10 pts] On the axes provided, sketch carefully requested quantity from $x = -x_M$ to x_B for $V_{GB} = 0$ V. Do not extend your sketch into the contacts. Assume the lightly doped p-region is fully depleted.

- i) The electric field, $E(x)$. Identify important values, e.g. $E(0^-)/E(0^+)$.



- ii) The charge density $\rho(x)$. Use Q'_p , Q'_n , and N_A to label your plot



Problem 3 continues on the next page

Problem 3 continued

- e) [5 pts] For $V_{GB}=0$ V, derive an expression for Q_p' and find its value. To simplify your calculation assume that the contribution to the charge density profile from the depleted acceptors in the lightly doped p-region between $x = 0$ and $x = X_A$ is negligible (that is, assume N_A is effectively zero).

$$Q_p' = \text{_____} = \text{_____} \text{ Coul/cm}^2$$

- f) [4 pts] Justify the assumption made in Part (e) that the charge in the depleted lightly doped p-region is negligible.

End of Problem 3; End of Exam

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