

6.012 Microelectronic Devices and Circuits

Formula Sheet for Exam Two, Fall 2009

Parameter Values:

$$\begin{aligned} q &= 1.6 \times 10^{-19} \text{ Coul} \\ \epsilon_0 &= 8.854 \times 10^{-14} \text{ F/cm} \\ \epsilon_{r,\text{Si}} &= 11.7, \quad \epsilon_{s,\text{Si}} \approx 10^{-12} \text{ F/cm} \\ n_i[\text{Si}@R.T] &\approx 10^{10} \text{ cm}^{-3} \\ kT/q &\approx 0.025 \text{ V}; \quad (kT/q) \ln 10 \approx 0.06 \text{ V} \\ 1 \mu\text{m} &= 1 \times 10^{-4} \text{ cm} \end{aligned}$$

Periodic Table:

	<u>III</u>	<u>IV</u>	<u>V</u>
	B	C	N
	Al	Si	P
	Ga	Ge	As
	In	Sn	Sb

Drift/Diffusion:

Drift velocity :	$\bar{s}_x = \pm \mu_m E_x$	$\epsilon \frac{dE(x)}{dx} = \rho(x)$	$E(x) = \frac{1}{\epsilon} \int \rho(x) dx$
Conductivity :	$\sigma = q(\mu_e n + \mu_h p)$	$-\frac{d\phi(x)}{dx} = E(x)$	$\phi(x) = - \int E(x) dx$
Diffusion flux :	$F_m = -D_m \frac{\partial C_m}{\partial x}$	$-\epsilon \frac{d^2 \phi(x)}{dx^2} = \rho(x)$	$\phi(x) = -\frac{1}{\epsilon} \iint \rho(x) dx dx$
Einstein relation :	$\frac{D_m}{\mu_m} = \frac{kT}{q}$		

Electrostatics:The Five Basic Equations:

Electron continuity :	$\frac{\partial n(x,t)}{\partial t} - \frac{1}{q} \frac{\partial J_e(x,t)}{\partial x} = g_L(x,t) - [n(x,t) \cdot p(x,t) - n_i^2] r(T)$
Hole continuity :	$\frac{\partial p(x,t)}{\partial t} + \frac{1}{q} \frac{\partial J_h(x,t)}{\partial x} = g_L(x,t) - [n(x,t) \cdot p(x,t) - n_i^2] r(T)$
Electron current density :	$J_e(x,t) = q\mu_e n(x,t) E(x,t) + qD_e \frac{\partial n(x,t)}{\partial x}$
Hole current density :	$J_h(x,t) = q\mu_h p(x,t) E(x,t) - qD_h \frac{\partial p(x,t)}{\partial x}$
Poisson's equation :	$\frac{\partial E(x,t)}{\partial x} = \frac{q}{\epsilon} [p(x,t) - n(x,t) + N_d^+(x) - N_a^-(x)]$

Uniform doping, full ionization, TEn - type, $N_d \gg N_a$

$$n_o \approx N_d - N_a \equiv N_D, \quad p_o = n_i^2 / n_o, \quad \phi_n = \frac{kT}{q} \ln \frac{N_D}{n_i}$$

p - type, $N_a \gg N_d$

$$p_o \approx N_a - N_d \equiv N_A, \quad n_o = n_i^2 / p_o, \quad \phi_p = -\frac{kT}{q} \ln \frac{N_A}{n_i}$$

Uniform optical excitation, uniform doping

$$n = n_o + n' \quad p = p_o + p' \quad n' = p' \quad \frac{dn'}{dt} = g_l(t) - (p_o + n_o + n') n' r$$

$$\text{Low level injection, } n', p' \ll p_o + n_o : \quad \frac{dn'}{dt} + \frac{n'}{\tau_{\min}} = g_l(t) \quad \text{with} \quad \tau_{\min} \approx (p_o r)^{-1}$$

Flow problems (uniformly doped quasineutral regions with quasi-static excitation and low level injection; p-type example):

$$\text{Minority carrier excess: } \frac{d^2 n'(x)}{dx^2} - \frac{n'(x)}{L_e^2} = -\frac{1}{D_e} g_L(x) \quad L_e \equiv \sqrt{D_e \tau_e}$$

$$\text{Minority carrier current density: } J_e(x) \approx q D_e \frac{dn'(t)}{dx}$$

$$\text{Majority carrier current density: } J_h(x) = J_{Tot} - J_e(x)$$

$$\text{Electric field: } E_x(x) \approx \frac{1}{q \mu_h p_o} \left[J_h(x) + \frac{D_h}{D_e} J_e(x) \right]$$

$$\text{Majority carrier excess: } p'(x) \approx n'(x) + \frac{\epsilon}{q} \frac{dE_x(x)}{dx}$$

Short base, infinite lifetime limit:

$$\text{Minority carrier excess: } \frac{d^2 n'(x)}{dx^2} \approx -\frac{1}{D_e} g_L(x), \quad n'(x) \approx -\frac{1}{D_e} \iint g_L(x) dx dx$$

Non-uniformly doped semiconductor sample in thermal equilibrium

$$\frac{d^2 \phi(x)}{dx^2} = \frac{q}{\epsilon} \{ n_i [e^{q\phi(x)/kT} - e^{-q\phi(x)/kT}] - [N_d(x) - N_a(x)] \}$$

$$n_o(x) = n_i e^{q\phi(x)/kT}, \quad p_o(x) = n_i e^{-q\phi(x)/kT}, \quad p_o(x) n_o(x) = n_i^2$$

Depletion approximation for abrupt p-n junction:

$$\rho(x) = \begin{cases} 0 & \text{for } x < -x_p \\ -qN_{Ap} & \text{for } -x_p < x < 0 \\ qN_{Dn} & \text{for } 0 < x < x_n \\ 0 & \text{for } x_n < x \end{cases} \quad N_{Ap} x_p = N_{Dn} x_n$$

$$\phi_b = \phi_n - \phi_p = \frac{kT}{q} \ln \frac{N_{Dn} N_{Ap}}{n_i^2}$$

$$w(v_{AB}) = \sqrt{\frac{2\epsilon_{Si}(\phi_b - v_{AB})(N_{Ap} + N_{Dn})}{q N_{Ap} N_{Dn}}} \quad |E_{pk}| = \sqrt{\frac{2q(\phi_b - v_{AB})}{\epsilon_{Si}} \frac{N_{Ap} N_{Dn}}{(N_{Ap} + N_{Dn})}}$$

$$q_{DP}(v_{AB}) = -A q N_{Ap} x_p (v_{AB}) = -A \sqrt{2q\epsilon_{Si}(\phi_b - v_{AB}) \frac{N_{Ap} N_{Dn}}{(N_{Ap} + N_{Dn})}}$$

Ideal p-n junction diode i-v relation (large signal model):

$$n(-x_p) = \frac{n_i^2}{N_{Ap}} e^{qv_{AB}/kT}, \quad n'(-x_p) = \frac{n_i^2}{N_{Ap}} (e^{qv_{AB}/kT} - 1); \quad p(x_n) = \frac{n_i^2}{N_{Dn}} e^{qv_{AB}/kT}, \quad p'(x_n) = \frac{n_i^2}{N_{Dn}} (e^{qv_{AB}/kT} - 1)$$

$$i_D = A q n_i^2 \left[\frac{D_h}{N_{Dn} w_{n,eff}} + \frac{D_e}{N_{Ap} w_{p,eff}} \right] \left[e^{qv_{AB}/kT} - 1 \right] \quad w_{m,eff} = \begin{cases} w_m - x_m & \text{if } L_m >> w_m \\ L_m \tanh[(w_m - x_m)/L_m] & \text{if } L_m \sim w_m \\ L_m & \text{if } L_m << w_m \end{cases}$$

$$q_{QNR,p-side} = A q \int_{-w_p}^{-x_p} n'(x) dx, \quad q_{QNR,n-side} = A q \int_{x_n}^{w_n} p'(x) dx, \quad \text{Note: } p'(x) \approx n'(x) \text{ in QNRs}$$

Large signal BJT Model in Forward Active Region (FAR):
(npn with base width modulation)

$$i_B(v_{BE}, v_{CE}) = I_{BS} \left(e^{qv_{BE}/kT} - 1 \right)$$

$$i_C(v_{BE}, v_{BC}) = \beta_F i_B(v_{BE}, v_{CE}) [1 + \lambda v_{CE}] = \beta_F I_{BS} \left(e^{qv_{BE}/kT} - 1 \right) [1 + \lambda v_{CE}]$$

$$\text{with : } I_{BS} \equiv \frac{I_{ES}}{(\beta_F + 1)} = \frac{Aqn_i^2}{(\beta_F + 1)} \left(\frac{D_h}{N_{DE}w_{E,eff}} + \frac{D_e}{N_{AB}w_{B,eff}} \right), \quad \beta_F \equiv \frac{\alpha_F}{(1 - \alpha_F)}, \text{ and } \lambda \equiv \frac{1}{V_A}$$

$$\text{Also, } \alpha_F = \frac{(1 - \delta_B)}{(1 + \delta_E)} \quad \text{and} \quad \beta_F \approx \frac{(1 - \delta_B)}{(\delta_E + \delta_B)} \quad \text{with} \quad \delta_E = \frac{D_h}{D_e} \cdot \frac{N_{AB}}{N_{DE}} \cdot \frac{w_{B,eff}}{w_{E,eff}} \quad \text{and} \quad \delta_B = \frac{w_{B,eff}^2}{2L_{eB}^2}$$

$$\text{When } \delta_B \approx 0 \quad \text{then} \quad \alpha_F \approx \frac{1}{(1 + \delta_E)} \quad \text{and} \quad \beta_F \approx \frac{1}{\delta_E}$$

MOS Capacitor:

$$\text{Flat - band voltage : } V_{FB} \equiv v_{GB} \text{ at which } \phi(0) = \phi_{p-Si} \quad [\Delta\phi = 0 \text{ in Si}]$$

$$V_{FB} = \phi_{p-Si} - \phi_m$$

$$\text{Threshold voltage : } V_T \equiv v_{GC} \text{ at which } \phi(0) = -\phi_{p-Si} - v_{BC} \quad [\Delta\phi = |2\phi_{p-Si}| - v_{BC} \text{ in Si}]$$

$$V_T(v_{BC}) = V_{FB} - 2\phi_{p-Si} + \frac{1}{C_{ox}^*} \left\{ 2\varepsilon_{Si} q N_A [|2\phi_{p-Si}| - v_{BC}] \right\}^{1/2}$$

$$\text{Depletion region width at threshold : } x_{DT}(v_{BC}) = \sqrt{\frac{2\varepsilon_{Si} [|2\phi_{p-Si}| - v_{BC}]}{q N_A}}$$

$$\text{Oxide capacitance per unit area : } C_{ox}^* = \frac{\varepsilon_{ox}}{t_{ox}} \quad [\varepsilon_{r,SiO_2} = 3.9, \quad \varepsilon_{SiO_2} \approx 3.5 \times 10^{-13} F/cm]$$

$$\text{Inversion layer sheet charge density : } q_N^* = -C_{ox}^* [v_{GC} - V_T(v_{BC})]$$

$$\text{Accumulation layer sheet charge density : } q_P^* = -C_{ox}^* [v_{GB} - V_{FB}]$$

Gradual Channel Approximation for MOSFET Characteristics:

(n-channel; strong inversion; with channel length modulation; no velocity saturation)
Only valid for $v_{BS} \leq 0, v_{DS} \geq 0$.

$$i_G(v_{GS}, v_{DS}, v_{BS}) = 0, \quad i_B(v_{GS}, v_{DS}, v_{BS}) = 0$$

$$i_D(v_{GS}, v_{DS}, v_{BS}) = \begin{cases} 0 & \text{for } \frac{1}{\alpha} [v_{GS} - V_T(v_{BS})] < 0 < v_{DS} \\ \frac{K_o}{2\alpha} [v_{GS} - V_T(v_{BS})]^2 [1 + \lambda(v_{DS} - v_{DS,sat})] & \text{for } 0 < \frac{1}{\alpha} [v_{GS} - V_T(v_{BS})] < v_{DS} \\ K_o \left\{ v_{GS} - V_T(v_{BS}) - \alpha \frac{v_{DS}}{2} \right\} v_{DS} & \text{for } 0 < v_{DS} < \frac{1}{\alpha} [v_{GS} - V_T(v_{BS})] \end{cases}$$

$$\text{with } V_T(v_{BS}) \equiv V_{FB} - 2\phi_{p-Si} + \frac{1}{C_{ox}^*} \left\{ 2\varepsilon_{Si} q N_A [|2\phi_{p-Si}| - v_{BS}] \right\}^{1/2}, \quad v_{DS,sat} \equiv \frac{1}{\alpha} [v_{GS} - V_T(v_{BS})]$$

$$K_o \equiv \frac{W}{L} \mu_e C_{ox}^*, \quad C_{ox}^* \equiv \frac{\varepsilon_{ox}}{t_{ox}}, \quad \alpha \equiv 1 + \frac{1}{C_{ox}^*} \left\{ \frac{\varepsilon_{Si} q N_A}{2 [|2\phi_{p-Si}| - v_{BS}]} \right\}^{1/2}, \quad \lambda \equiv \frac{1}{V_A}$$

Large Signal Model for MOSFETs Operated Sub-Threshold (weak inversion):
(n-channel) Only valid for $v_{GS} \leq V_T$, $v_{DS} \geq 0$, $v_{BS} \leq 0$.

$$i_G(v_{GS}, v_{DS}, v_{BS}) = 0, \quad i_B(v_{GS}, v_{DS}, v_{BS}) \approx 0$$

$$i_{D,s-t}(v_{GS}, v_{DS}, v_{BS}) \approx I_{S,s-t} e^{q\{v_{GS}-V_T(v_{BS})\}/n kT} \left(1 - e^{-qv_{DS}/kT}\right) \text{ where } I_{S,s-t} = \frac{W}{2L} \mu_e \left(\frac{kT}{q}\right)^2 \sqrt{\frac{2\varepsilon_{Si}qN_A}{|2\phi_p| - v_{BS}}} = \frac{K_o V_t^2 \gamma}{2\sqrt{|2\phi_p| - v_{BS}}}$$

$$\text{with } V_t = \frac{kT}{q}, \quad K_o = \frac{W}{L} \mu_e C_{ox}^*, \quad \gamma = \frac{\sqrt{2\varepsilon_{Si}qN_A}}{C_{ox}^*}, \quad n \approx 1 + \frac{\gamma}{2\sqrt{|2\phi_p| - v_{BS}}}$$

Large Signal Model for MOSFETs Reaching Velocity Saturation at Small v_{DS} :
(n-channel) Only valid for $v_{BS} \leq 0$, $v_{DS} \geq 0$. Neglects $v_{DS}/2$ relative to $(v_{GS}-V_T)$.

$$\text{Saturation model: } s_y(E_y) = \mu_e E_y \text{ if } E_y \leq E_{crit}, \quad s_y(E_y) = \mu_e E_{crit} \equiv s_{sat} \text{ if } E_y \geq E_{crit}$$

$$i_G(v_{GS}, v_{DS}, v_{BS}) = 0, \quad i_B(v_{GS}, v_{DS}, v_{BS}) = 0$$

$$i_D(v_{GS}, v_{DS}, v_{BS}) \approx \begin{cases} 0 & \text{for } (v_{GS} - V_T) < 0 < v_{DS} \\ W s_{sat} C_{ox}^* [v_{GS} - V_T(v_{BS})] [1 + \lambda(v_{DS} - E_{crit}L)] & \text{for } 0 < (v_{GS} - V_T), E_{crit}L < v_{DS} \\ \frac{W}{L} \mu_e C_{ox}^* [v_{GS} - V_T(v_{BS})] v_{DS} & \text{for } 0 < (v_{GS} - V_T), v_{DS} < E_{crit}L \end{cases}$$

$$\text{with } \lambda = 1/V_A$$

CMOS Performance

Transfer characteristic:

$$\text{In general: } V_{LO} = 0, \quad V_{HI} = V_{DD}, \quad I_{ON} = 0, \quad I_{OFF} = 0$$

$$\text{Symmetry: } V_M = \frac{V_{DD}}{2} \text{ and } NM_{LO} = NM_{HI} \Rightarrow K_n = K_p \text{ and } |V_{Tp}| = V_{Tn}$$

$$\text{Minimum size gate: } L_n = L_p = L_{min}, \quad W_n = W_{min}, \quad W_p = (\mu_n/\mu_p)W_n \quad [\text{or } W_p = (s_{sat,n}/s_{sat,p})W_n]$$

Switching times and gate delay (no velocity saturation):

$$\tau_{Charg e} = \tau_{Disch arg e} = \frac{2C_L V_{DD}}{K_n [V_{DD} - V_{Tn}]^2}$$

$$C_L = n(W_n L_n + W_p L_p) C_{ox}^* = 3n W_{min} L_{min} C_{ox}^* \quad \text{assumes } \mu_e = 2\mu_h$$

$$\tau_{Min.Cycle} = \tau_{Charg e} + \tau_{Disch arg e} = \frac{12nL_{min}^2 V_{DD}}{\mu_e [V_{DD} - V_{Tn}]^2}$$

Dynamic power dissipation (no velocity saturation):

$$P_{dyn@f_{max}} = C_L V_{DD}^2 f_{max} \propto \frac{C_L V_{DD}^2}{\tau_{Min.Cycle}} \propto \frac{\mu_e W_{min} \varepsilon_{ox} V_{DD} [V_{DD} - V_{Tn}]^2}{t_{ox} L_{min}}$$

$$PD_{dyn@f_{max}} = \frac{P_{dyn@f_{max}}}{\text{InverterArea}} \propto \frac{P_{dyn@f_{max}}}{W_{min} L_{min}} \propto \frac{\mu_e \varepsilon_{ox} V_{DD} [V_{DD} - V_{Tn}]^2}{t_{ox} L_{min}^2}$$

Switching times and gate delay (full velocity saturation):

$$\begin{aligned}\tau_{Ch \arg e} &= \tau_{Disch \arg e} = \frac{C_L V_{DD}}{W_{\min} S_{sat} C_{ox}^* [V_{DD} - V_{Tn}]} \\ C_L &= n(W_n L_n + W_p L_p) C_{ox}^* = 2n W_{\min} L_{\min} C_{ox}^* \quad \text{assumes } s_{sat,e} = s_{sat,h} \\ \tau_{Min.Cycle} &= \tau_{Ch \arg e} + \tau_{Disch \arg e} = \frac{4nL_{\min} V_{DD}}{S_{sat} [V_{DD} - V_{Tn}]}\end{aligned}$$

Dynamic power dissipation per gate (full velocity saturation):

$$\begin{aligned}P_{dyn @ f_{\max}} &= C_L V_{DD}^2 f_{\max} \propto \frac{C_L V_{DD}^2}{\tau_{Min.Cycle}} \propto \frac{S_{sat} W_{\min} \epsilon_{ox} V_{DD} [V_{DD} - V_{Tn}]}{t_{ox}} \\ PD_{dyn @ f_{\max}} &= \frac{P_{dyn @ f_{\max}}}{\text{InverterArea}} \propto \frac{P_{dyn @ f_{\max}}}{W_{\min} L_{\min}} \propto \frac{S_{sat} \epsilon_{ox} V_{DD} [V_{DD} - V_{Tn}]}{t_{ox} L^2}\end{aligned}$$

Static power dissipation per gate

$$\begin{aligned}P_{static} &= V_{DD} I_{D,off} \approx V_{DD} \frac{W_{\min}}{L_{\min}} \mu_e V_t^2 \sqrt{\frac{\epsilon_{Si} q N_A}{2 |V_{BS}|}} e^{\{-V_T\}/nV_t} \\ PD_{static} &= \frac{P_{static}}{\text{Inverter Area}} \propto \frac{V_{DD}}{L_{\min}^2} \mu_e V_t^2 \sqrt{\frac{\epsilon_{Si} q N_A}{2 |V_{BS}|}} e^{\{-V_T\}/nV_t}\end{aligned}$$

CMOS Scaling Rules - Constant electric field scaling

Scaled Dimensions: $L_{\min} \rightarrow L_{\min}/s$ $W \rightarrow W/s$ $t_{ox} \rightarrow t_{ox}/s$ $N_A \rightarrow sN_A$

Scaled Voltages: $V_{DD} \rightarrow V_{DD}/s$ $V_{BS} \rightarrow V_{BS}/s$

Consequences: $C_{ox}^* \rightarrow sC_{ox}^*$ $K \rightarrow sK$ $V_T \rightarrow V_T/s$

$\tau \rightarrow \tau/s$ $P_{dyn} \rightarrow P_{dyn}/s^2$ $PD_{dyn @ f_{\max}} \rightarrow PD_{dyn @ f_{\max}}$

$PD_{static} \rightarrow s^2 e^{(s-1)V_T/snV_t} PD_{static}$

Device transit times

$$\text{Short Base Diode transit time: } \tau_b = \frac{w_B^2}{2D_{\min,B}} = \frac{w_B^2}{2\mu_{\min,B} V_{thermal}}$$

$$\text{Channel transit time w.o. velocity saturation: } \tau_{Ch} = \frac{2}{3} \frac{L^2}{\mu_{Ch} |V_{GS} - V_T|}$$

$$\text{Channel transit time with velocity saturation: } \tau_{Ch} = \frac{L}{s_{sat}}$$

Small Signal Linear Equivalent Circuits:

- p-n Diode (n^+ -p doping assumed for C_d)

$$g_d \equiv \left. \frac{\partial i_D}{\partial v_{AB}} \right|_Q = \frac{q}{kT} I_S e^{qV_{AB}/kT} \approx \frac{qI_D}{kT}, \quad C_d = C_{dp} + C_{df},$$

where $C_{dp}(V_{AB}) = A \sqrt{\frac{q\varepsilon_{Si}N_{Ap}}{2(\phi_b - V_{AB})}}$, and $C_{df}(V_{AB}) = \frac{qI_D}{kT} \frac{[w_p - x_p]^2}{2D_e} = g_d \tau_d$ with $\tau_d \equiv \frac{[w_p - x_p]^2}{2D_e}$

- BJT (in FAR)

$$g_m = \frac{q}{kT} \beta_o I_{BS} e^{qV_{BE}/kT} [1 + \lambda V_{CE}] \approx \frac{qI_C}{kT}, \quad g_\pi = \frac{g_m}{\beta_o} = \frac{qI_C}{\beta_o kT}$$

$$g_o = \beta_o I_{BS} [e^{qV_{BE}/kT} + 1] \lambda \approx \lambda I_C \quad \left(\text{or } \approx \frac{I_C}{V_A} \right)$$

$$C_\pi = g_m \tau_b + \text{B-E depletion cap. with } \tau_b \equiv \frac{w_B^2}{2D_e}, \quad C_\mu : \text{B-C depletion cap.}$$

- MOSFET (strong inversion; in saturation, no velocity saturation)

$$g_m = K [V_{GS} - V_T(V_{BS})] [1 + \lambda V_{DS}] \approx \sqrt{2KI_D}$$

$$g_o = \frac{K}{2} [V_{GS} - V_T(V_{BS})]^2 \lambda \approx \lambda I_D \quad \left(\text{or } \approx \frac{I_D}{V_A} \right)$$

$$g_{mb} = \eta g_m = \eta \sqrt{2KI_D} \quad \text{with } \eta \equiv - \left. \frac{\partial V_T}{\partial v_{BS}} \right|_Q = \frac{1}{C_{ox}^*} \sqrt{\frac{\varepsilon_{Si} q N_A}{|q\phi_p| - V_{BS}}}$$

$$C_{gs} = \frac{2}{3} W L C_{ox}^*, \quad C_{sb}, C_{gb}, C_{db} : \text{depletion capacitances}$$

$C_{gd} = W C_{gd}^*$, where C_{gd}^* is the G-D fringing and overlap capacitance per unit gate length (parasitic)

- MOSFET (strong inversion; in saturation with full velocity saturation)

$$g_m = W s_{sat} C_{ox}^*, \quad g_o = \lambda I_D = \frac{I_D}{V_A}, \quad g_{mb} = \eta g_m \quad \text{with } \eta \equiv - \left. \frac{\partial V_T}{\partial v_{BS}} \right|_Q = \frac{1}{C_{ox}^*} \sqrt{\frac{\varepsilon_{Si} q N_A}{|q\phi_p| - V_{BS}}}$$

$$C_{gs} = W L C_{ox}^*, \quad C_{sb}, C_{gb}, C_{db} : \text{depletion capacitances}$$

$C_{gd} = W C_{gd}^*$, where C_{gd}^* is the G-D fringing and overlap capacitance per unit gate length (parasitic)

- MOSFET (operated sub-threshold; in forward active region; only valid for $v_{bs} = 0$)

$$g_m = \frac{qI_D}{n kT}, \quad g_o = \lambda I_D = \frac{I_D}{V_A}$$

$$C_{gs} = W L C_{ox}^* \sqrt{1 + \frac{2C_{ox}^{*2}(V_{GS} - V_{FB})}{\varepsilon_{Si} q N_A}}, \quad C_{db} : \text{drain region depletion capacitance}$$

$C_{gd} = W C_{gd}^*$, where C_{gd}^* is the G-D fringing and overlap capacitance per unit gate length (parasitic)

MIT OpenCourseWare
<http://ocw.mit.edu>

6.012 Microelectronic Devices and Circuits

Fall 2009

For information about citing these materials or our Terms of Use, visit: <http://ocw.mit.edu/terms>.