

**MASSACHUSETTS INSTITUTE OF TECHNOLOGY**  
*Department of Electrical Engineering and Computer Science*  
**6.012 Microelectronic Devices and Circuits – Fall 2009**

**SPECIAL PROBLEM ON CIRCUIT DESIGN – 12/1/09 edition**

**Issued:** Wednesday, November 18, 2009; updated Dec. 1.

**Due:** Friday, December 4, 2009 and on (be sure that your name is checked off the master list as you hand in your solution). Late solutions will receive zero points; see I.5 below.

**Updates:** Issues will be dealt with as needed; watch your e-mail.

**I. General Comments**

Do not panic when you see the circuit. It looks overwhelming at first but it is made up of simple building-block pieces and it is understandable. In addition, you will be given help along the way, first by this write-up, and later in recitations, lectures, and additional handouts. At the same time, the design process you need to go through is a complex one and it is not one you will successfully negotiate in one sitting. Thus it is important that you get started, first developing an understanding of the circuit and the nature of the design challenge, and then at doing your design. You can do it, but not in one night.

**II. The Ground Rules**

1. Consider this design problem more like an open book exam, than a problem set. You are encouraged to consult references and to seek guidance from the 6.012 staff, and to discuss design issues with others, but you should not work on your specific design and write-up with any other students or any other individuals. Nor should you compare design values or performance results with other students. The design you submit must be your own; any collaborations (and they should be minor) should be noted.
2. Do not let the design slide until the last week. Make a first attempt at a solution early so you can obtain any clarification and guidance you may need from the 6.012 staff before the Thanksgiving holiday (Nov. 26-29).
3. You are required to submit a completed Excel file cover sheet, and a detailed discussion of your design and your approach to arriving at it. The Excel file cover sheet will be available on Stellar. Your write-up should include circuit diagrams for your large signal and incremental analyses, and the equations you used and calculations you made. It should also include a discussion of the trade-offs you considered in your design. View the minimum performance objectives as a challenge and try to do even better.
4. Make reasonable approximations. Do not carry your calculations out to any more than three (3) significant figures. Your predicted performance values should also be stated to no more than three (3) significant figures. The following are examples of numbers with three significant figures: 1.23, 0.123, 123, 3450, 0.0345,  $6.78 \times 10^9$ .

5. Anyone who does not submit a design problem solution which demonstrates a reasonable level of effort will automatically receive zero points and a grade of "I" for 6.012 (as long as their performance is otherwise passing). An "I" received for this reason can only be completed by submitting an acceptable solution to this term's design problem by January 15, 2010. Late solutions will be checked to determine that they are acceptable, but will receive zero points for purposes of determining an overall course grade.

### III. Design Objective

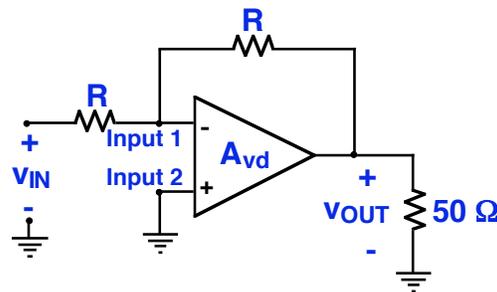
Your design objective is to specify transistor dimensions for the integrated linear amplifier shown in Figure 1 on Page 3 so that it meets or, hopefully, exceeds the performance objectives itemized below. You are able to increase MOSFET gate widths and/or lengths and BJT areas by integer multiples.

The circuit, which is described in full detail in Section V, is a BiCMOS differential amplifier designed to have a large differential-mode gain, large common-mode rejection ratio, large common mode input voltage range, and large output voltage swing.

You are to specify the dimensions of the devices in the circuit in Figure 1, and to calculate the corresponding bias levels and performance characteristics. You are also expected to discuss the main aspects of your design in your solution write-up, and to also discuss there the factors you took into consideration in arriving at your design.

*Performance Objectives:*

- 1) Small signal gains defined by writing  $v_{out} = A_{vc}(v_{in1} + v_{in2})/2 + A_{vd}(v_{in1} - v_{in2})$ 
  - a) Small-signal differential-mode voltage gain,  $A_{vd}$ , into a  $50\ \Omega$  load: as large as possible, and not less than 125,000
  - b) Small-signal common-mode voltage gain,  $A_{vc}$ , into a  $50\ \Omega$  load: as small as possible, and not more than 0.002
- 2) Common-mode rejection ratio,  $A_{vd}/A_{vc} : \geq 5 \times 10^7$
- 3) Small-signal output resistance,  $r_{out} : \leq 10\ \Omega$ .
- 4) Maximum output voltage swing into a  $50\ \Omega$  load,  $|v_{OUT}|_{max} : \geq 0.75\ V$ .
- 5) Minimum common-mode input voltage range,  $|v_{IC}|_{min} : \geq 0.75\ V$ .
- 6) Total quiescent power dissipation not to exceed 8.5 mW.
- 7) Output Voltage, i.e. the quiescent voltage at the output, i.e.  $v_{OUT}$ , when  $v_{IN} = 0$ , in a feedback circuit like that illustrated to the right assuming perfect element matching:  $|V_{OUT}| \leq 20\ \mu V$ .



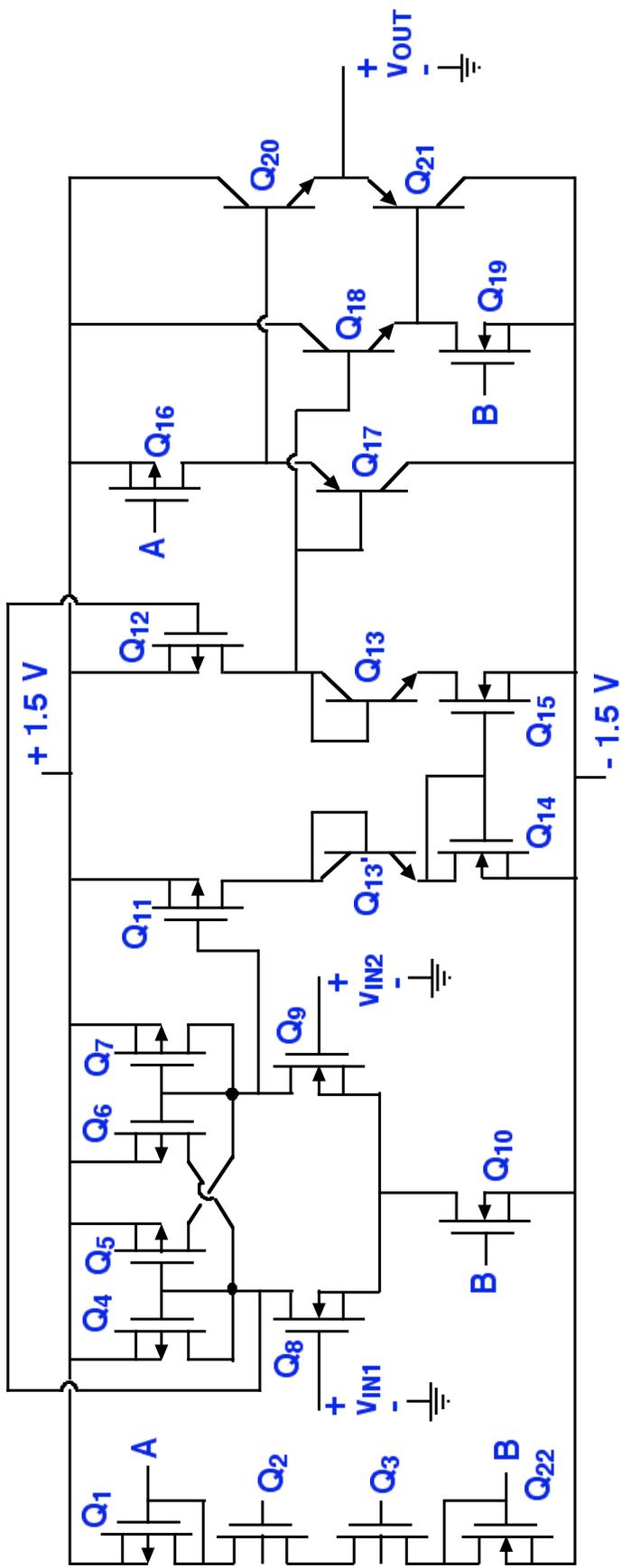


Figure 1 - The Fall 2009 Design Problem circuit, a high gain BICMOS differential amplifier with enhanced common-mode rejection ratio.

## IV. Component Specifications

### A. *Transistors*

All of the MOSFETs in this amplifier should be operated in strong inversion (as opposed to sub-threshold). Some of the transistors in the circuit can be chosen to be the smallest devices that can be made with the fabrication process used, but others will have to be designed to be larger; this might be done to adjust the value of a current source, for example, or to maximize the gain of a stage. In the listing below the properties of the minimum size devices are listed first and then the scaling rules for designing larger devices are given.

1. npn Bipolar Transistors -- The npn transistors are vertical structures that have the following large-signal and small-signal (hybrid- $\pi$ ) parameters

a) *Minimum size devices*

- i)  $\beta_F = 200$
- ii)  $I_C = 100 \mu\text{A}$  when  $V_{BE} = 0.6 \text{ V}$  (i.e.  $I_{ES} = 10^{-14} \text{ A}$ )  
 $V_{CE,sat} = 0.3 \text{ V}$
- iii)  $g_m = qI_C/kT$ ,  $g_\pi = g_m/\beta_F$   
 $g_o = I_C/|V_A|$  with  $|V_A| = 50\text{V}$
- iv) Operating range:  $1.0 \mu\text{A} \leq I_C \leq 3 \text{ mA}$

b) *Scaled devices* -- You may increase the base-emitter junction area by up to a factor of 25 times. Increasing the base-emitter junction area,  $A_E$ , by a factor of  $\gamma$ , increases the current limits on the operating range by the same factor. The emitter-base diode saturation current in the Ebers-Moll model,  $I_{ES}$ , increases by the same factor,  $\gamma$ ; so too does  $I_{CS}$ . No other static model parameters change.

2. pnp Bipolar Transistors -- The pnp transistors are lateral structures that have the following large-signal and small-signal (hybrid- $\pi$ ) parameters

a) *Minimum size devices*

- i)  $\beta_F = 100$
- ii)  $I_C = -100 \mu\text{A}$  when  $V_{BE} = -0.6 \text{ V}$  (i.e.  $I_{ES} = 10^{-14} \text{ A}$ )  
 $V_{CE,sat} = -0.3 \text{ V}$
- iii)  $g_m = q|I_C|/kT$ ,  $g_\pi = g_m/\beta_F$   
 $g_o = |I_C|/|V_A|$  with  $|V_A| = 50\text{V}$
- iv) Operating range:  $0.5 \mu\text{A} \leq I_C \leq 1.5 \text{ mA}$

b) *Scaled devices* -- You may increase the base-emitter junction area by up to a factor of 25 times. Increasing the base-emitter junction area,  $A_E$ , by a factor of  $\gamma$ , increases the current limits on the operating range by the same factor. The emitter-base diode saturation current in the Ebers-Moll model,  $I_{ES}$ , increases by the same factor,  $\gamma$ ; so too does  $I_{CS}$ . No other static model parameters change.

3. n-channel MOSFET's -- The n-channel MOSFET's are enhancement-mode devices with the following large and small-signal parameters.

- a) *Minimum size devices* ( $W = W_{min}$ ,  $L = L_{min}$ )
- i)  $K = 5.0 \text{ mA/V}^2$        $\alpha = 1$
  - ii)  $V_T = +0.4 \text{ V}$
  - iii)  $g_m = K(V_{GS} - V_T) = (2KI_D)^{1/2} = 2I_D / (V_{GS} - V_T)$   
 $g_o = \lambda I_D = I_D / |V_A|$  with  $|V_A| = 10 \text{ V}$
  - iv) Operating range:  $(V_{GS} - V_T) \geq 0.1 \text{ V}$

b) *Scaled devices* -- The width of the gate (and channel),  $W$ , can be as large as  $150 W_{min}$  and the length can be long as  $4 L_{min}$ . The magnitude of the Early voltage increases linearly with  $L$ .

4. p-channel MOSFET's -- The p-channel MOSFET's are enhancement-mode devices with the following large and small-signal parameters.

- a) *Minimum size devices* ( $W = W_{min}$ ,  $L = L_{min}$ )
- i)  $K = 2.5 \text{ mA/V}^2$        $\alpha = 1$
  - ii)  $V_T = -0.4 \text{ V}$
  - iii)  $g_m = K(V_{SG} - |V_T|) = (2K|I_D|)^{1/2} = 2|I_D| / (V_{SG} - |V_T|)$   
 $g_o = \lambda |I_D| = |I_D| / |V_A|$  with  $|V_A| = 10 \text{ V}$
  - iv) Operating range:  $(V_{SG} - |V_T|) \geq 0.1 \text{ V}$

b) *Scaled devices* -- The width of the gate (and channel),  $W$ , can be as large as  $150 W_{min}$  and the length can be long as  $4 L_{min}$ . The magnitude of the Early voltage increases linearly with  $L$ .

## B. Power Supplies

The power supplies are ideal voltage sources with fixed values of 1.5 V and -1.5 V relative to ground.

## V. Discussion of the Circuit

You should first look at the circuit carefully and identify its various pieces. Initially the circuit looks very complicated but if you break it into its component parts and understand what each does and how they interact, you will find that the amplifier is actually much less formidable.

Begin by identifying the biasing circuitry and the current sources, in this case three n-channel MOSFETs ( $Q_{10}$ ,  $Q_{19}$ , and  $Q_{22}$ ), two p-channel MOSFETs ( $Q_1$  and  $Q_{16}$ ), and two you can choose to make either n- or p-channel ( $Q_2$  and  $Q_3$ ; you must also specify where the gates and substrates of these two transistors are connected).

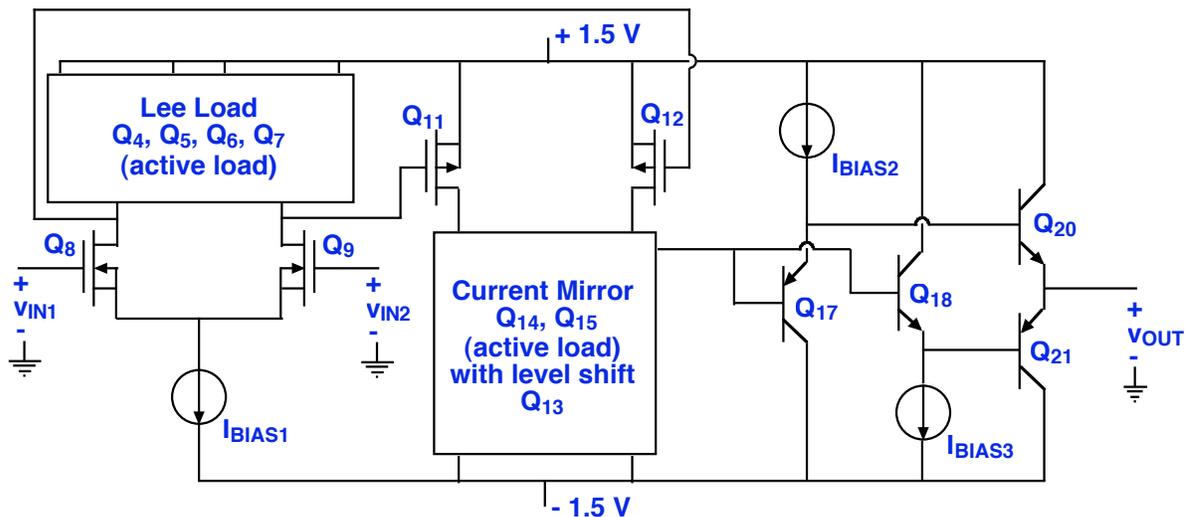
The chain formed by  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_{22}$  determines the voltages at points A and B, which are used to establish the gate-to-source voltages of transistors functioning as current sources,  $Q_{10}$ ,  $Q_{16}$ , and  $Q_{19}$ . Specifically,  $Q_{10}$  functions as a current source that directly biases the first stage (transistors  $Q_4$ ,  $Q_5$ ,  $Q_6$ ,  $Q_7$ ,  $Q_8$ ,

and  $Q_9$ ), and indirectly also biases the second stage (transistors  $Q_{11}$ ,  $Q_{12}$ ,  $Q_{13}$ ,  $Q_{13'}$ ,  $Q_{14}$ , and  $Q_{15}$ ). Transistors  $Q_{16}$  and  $Q_{19}$  function as current sources that are the stage loads (non-linear) of the pnp and npn BJT emitter follower stages containing transistors  $Q_{17}$  and  $Q_{18}$ , respectively; they also bias  $Q_{17}$  and  $Q_{18}$ .

Once you see which transistors are involved in current source biasing you can mentally replace them with current sources, as we will do in Figure 2, and ignore those devices initially, and until you have decided what levels of bias current you need.

Move on next to look at the amplifier stages, starting with the input stage,  $Q_8$  and  $Q_9$ . This stage is an n-channel MOSFET common-source differential stage, i.e., a source coupled pair, loaded with an active load called the Lee Load, after Professor Tom Lee of Stanford (a former 6.012 student) who invented it (not in 6.012). The Lee Load looks incrementally like a very large resistor for differential-mode inputs, and like a very much smaller resistor for common-mode inputs. The difference-mode voltage gain is thus very large and the common-mode voltage gain is less than one (i.e., it is not a gain, but an attenuation). Consequently using the Lee Load results in a gain stage with a large common-mode rejection ratio.

The second stage is a common source differential stage loaded with an active load called a current mirror. By using a p-MOS second gain stage it is possible to bias this stage directly from the first stage, rather than the more conventional way in differential circuits of using a current source to bias it. This increases the positive output voltage swing significantly, which is important in a circuit like this designed to run off only  $\pm 1.5$  V voltage supplies.



**Figure 2** - A simplified schematic of the design problem circuit drawing attention to some of the functional units of the circuit. There are four stages in this amplifier: From left to right, we find that Stage 1 is an n-MOS common-source gain stage with a p-MOS Lee Load; Stage 2 is a p-MOS common-source gain stage with an n-MOS current mirror load; Stage 3 is a pair of emitter-follower buffer stages; and Stage 4 is a bipolar push-pull output stage (this is essentially another emitter-follower stage).

The load of the second stage is an n-MOS current mirror load, and as such it does several things: First, it provides an active load which effectively applies the output of the  $Q_{11}$  to the gate of  $Q_{15}$ , so that the output due to the difference-mode signal input to  $Q_{11}$  is added to the output due to the difference-mode signal input to  $Q_{12}$ . Doing this converts the output from a double-ended (or differential) output to a single-ended output, and does so in such a manner that we obtain an additional factor of two in gain. (This is explained in Section 12.4, pages 392-395 in the Course Text.) Second, the current mirror load, like that of the Lee Load, looks different for difference-mode signals and common-mode signals. As a consequence the difference-mode gain of this stage is large. At the same time, the common mode gain of this stage is small.

The output of the second stage is taken from the node joining the drains of  $Q_{12}$  and  $Q_{15}$ . This node is what is called a “high impedance” node. Ideally the voltage on this node would match that on the node joining the drains of  $Q_{11}$  and  $Q_{14}$ , and the voltage on this latter node is known because it is connected to the gates of  $Q_{14}$  and  $Q_{15}$ . In this circuit you will find that the voltage on this node is much lower than it should be to achieve the specification that the quiescent output voltage,  $V_{OUT}$ , be 0 V. Consequently, the diode-connected BJTs,  $Q_{13}$  and  $Q_{13'}$ , have been inserted to increase the quiescent voltage drain of  $Q_{12}$  and the bases of  $Q_{17}$  and  $Q_{18}$ .

The goal is to increase the quiescent voltage drain of  $Q_{12}$  as much as possible without limiting the output voltage swing, but it is not possible, nor is it necessary, to make it high enough to itself yield  $V_{OUT} = 0$  V. In practice, the quiescent value of the voltage on the drain of  $Q_{12}$  is very sensitive to differences in the transistors and process variations, and as a practical matter it cannot be predicted with certainty. This is a very common situation in high gain differential amplifiers and the issue is dealt with by using the amplifier with feedback that stabilizes the quiescent output voltage very near to zero Volts. The practical consequence for your analysis is that you can assume that the quiescent output voltage is zero volts. You should then calculate how much of a differential bias voltage is needed at the input of your design to make  $V_{OUT} \approx 0$  V assuming perfect matching (this will be discussed in class).

The third “stage is a pair of emitter-follower stages, one that uses a pnp BJT and the other that uses an npn BJT. These followers are coupled to the fourth and final stage, which is a complementary output stage called a push-pull stage. This is basically an emitter-follower stage in which an npn bipolar transistor ( $Q_{20}$  in this circuit) drives the load (i.e., supplies current to the load resistor) when the output voltage goes above zero, and a pnp bipolar transistor ( $Q_{21}$ ) drives the load when the voltage goes negative. With zero output voltage, all four transistors are equally on. However, as the output signal goes positive the pnp transistors are turned off and the npn transistors turn on more strongly supplying current to the load through  $Q_{20}$ . When the output goes negative, the opposite happens and the pnp transistor,  $Q_{21}$ , turns on strongly drawing current through the load.

Taken together the last two stages give the amplifier a low output resistance and provide a buffer between the 50 Ohm load and the high gain second stage. (See Section 11.3.4, and especially the discussion on Page 345, in the Course Text. This is a different push-pull design than that in the text, but the basic idea is the same.) The interactions with the output stages and the second

gain stage are particularly important to consider: First,  $Q_{17}$  and  $Q_{18}$  should be sized and biased so that there is no bias current drawn from the second stage. You will find, in fact, that the relative sizes of all of the bipolar transistors ( $Q_{17}$ ,  $Q_{18}$ ,  $Q_{20}$ , and  $Q_{21}$ ) are important when designing the biasing. Second, the input resistance of the emitter follower stages loads the cascode gain stage and plays an important role in limiting the gain of that stage. Third, the output resistance of the amplifier is limited in part by the output resistance of the second gain stage. The bias currents set by  $Q_{20}$  and  $Q_{21}$  also play an important role in setting the output resistance and you will find that there is a clear trade-off between output resistance and quiescent power dissipation. All told, the output stages are perhaps the most interesting part of the circuit, as will become more clear as the design problem circuit is discussed in lecture, recitation, and tutorials.

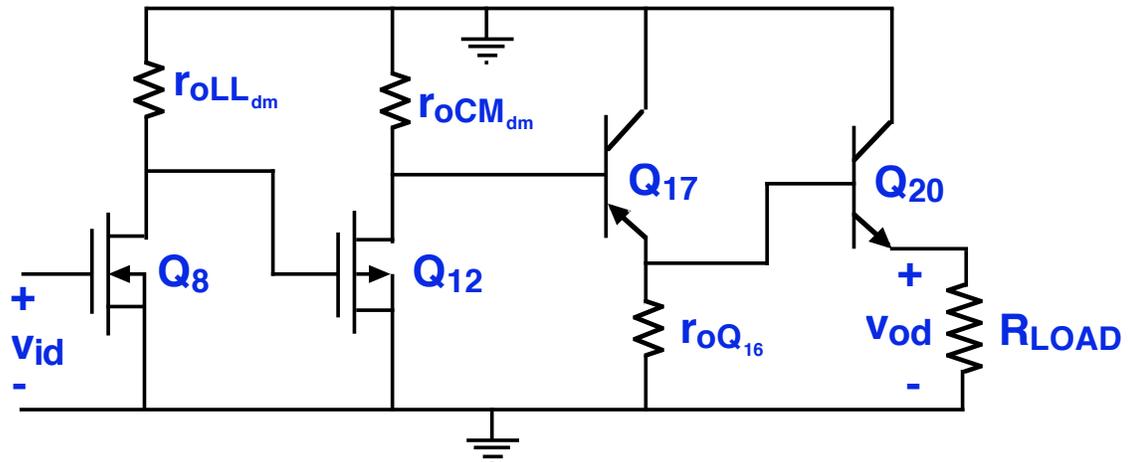
## VI. Starting your Analysis

As pointed out earlier, one of the first things to do is to identify the various sub-circuits in the full circuit, i.e., the various gain stages, the biasing circuitry, etc. Then look at each piece individually and understand what it can do and what constraints are placed upon it. Look at each gain stage, for example, and write an expression for its gain. Try to get a relationship that depends on the bias level and device parameters, and then on any bounds on the dimensions of the devices, and on any limitations on the operating currents and/or voltages of the devices. We know in general, for example, that MOSFET gain stages loaded with non-linear loads formed from transistors biased in their constant current regions (i.e., saturation in the case MOSFETs operated in strong inversion) tend to have higher gain when biased at low levels of drain current, that is, with small values of  $(|V_{GS}| - |V_T|)$ . Since there is a minimum value this quantity can have, it will be useful to try to express the gain of the current mirror gain stage in terms of  $(|V_{GS}| - |V_T|)_{\min}$  and find what the maximum gain for the stage can be. Then you can begin to understand how you must size and bias the stage to achieve that gain (or as near to it as possible).

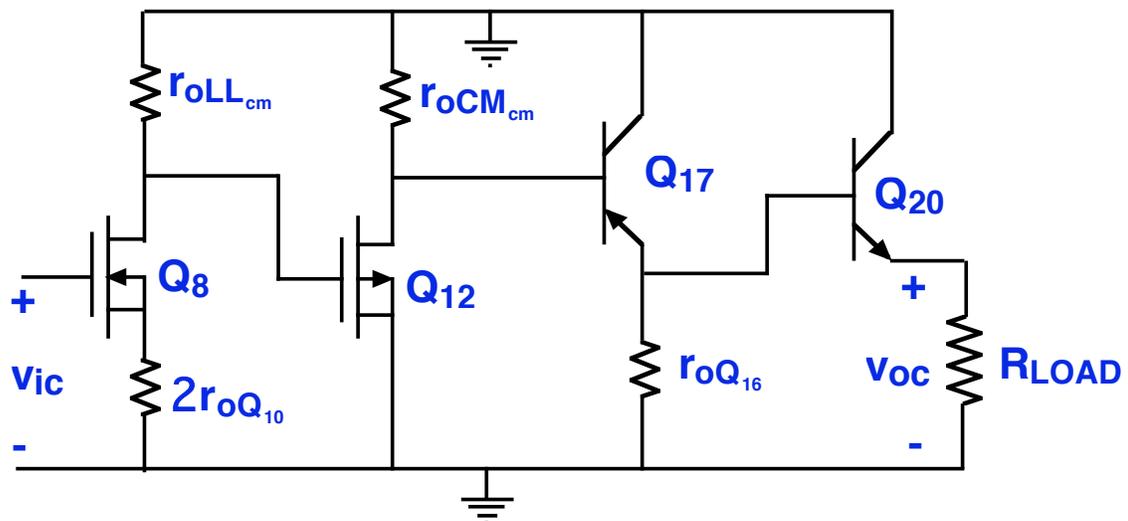
You should also spend some time understanding the output stages; in particular what the output resistance depends upon and whether that impacts any earlier stage(s), and what constraint the output voltage swing specification implies. To analyze the final stage you can assume that both of the transistors are active for your incremental modeling, whereas for your large signal analysis of the maximum output voltage swing, only one of these transistors will be on at a time.

To help you get started understanding the incremental behavior of the amplifier, partial small signal linear equivalent circuits for the amplifier with difference- and common-mode inputs respectively are shown in Figure 3a and 3b. You do not need to work out the effective resistances of the Lee and Current Mirror loads, but rather can use the gain expressions you will be given in class, but do make sure that you have all the factors of two correctly accounted for, etc. (i.e., don't apply the equations you are given blindly).

The biasing circuitry can be viewed as a separate issue in terms of understanding how it operates. Once you do this you can understand how to size the various transistors to achieve the bias levels you need based on your understanding and analysis of the amplifier proper. Of course, there may be limitations placed on the bias levels you can achieve that force you to adjust your



(a) Difference-mode input



(b) Common-mode input

**Figure 3** - Partial linear equivalent circuits for the design problem circuit for difference-mode and common-mode inputs. Notice that the p-MOS second stage and pnp third stage have been drawn with their transistors' source and emitter, respectively, down, whereas on the full schematic they are up. We can do this in the small signal linear equivalent circuit world because up and down are both ground (i.e., both the upper and lower rails are grounds). Notice also that the transistors and loads need to be replaced by their linear equivalent circuits to get the complete linear equivalent circuit of the amplifier, and the factor of 2 enhancement from the current mirror has to be included, but these abstractions help one gain insight.

designs for the amplifier stages, but by that point your understanding of the circuits should be such that making any such adjustments is not a major calamity; a major pain maybe, but no cause for panic.

A second set of things you should do early in your design process is to look through the design specifications and understand upon what each depends. As

you develop an understanding of the circuit, you can write expressions for the various quantities specified (i.e., voltage gains, input and output resistances, etc.).

Once you begin to understand the pieces and the specifications, make some initial design choices and see what you get. You may find that some parts work just fine, while others require major reworking. It may take several iterations to meet all of the specifications, but the more you understand the pieces and their interactions, and understand the implications for the circuit of the constraints placed on the sizes and operating ranges of the devices, the more quickly you can get to the answer and the less of a random walk your effort will seem.

## **VII. Enhancements to the Circuit**

You are, of course, encouraged to design your circuit to surpass the design performance specifications, particularly the gain specs, by as much as possible. In addition, you are encouraged to think about (and discuss in your write up) ways that the circuit could be improved beyond the present design, as well as why certain choices were not made in the design. You might want to consider, for example, using MOSFETs in the output stages, and discussing whether they offer performance advantages. You could consider using a cascode in the second gain stage, which would significantly increase the open circuit gain of that stage, but also considerably increase its output resistance.

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