

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.012 MICROELECTRONIC DEVICES AND CIRCUITS

Problem Set No. 7

Issued: October 21, 2009

Due: October 28, 2009

Reading Assignments:

Lecture 12 (10/22/09) - Notes

Lecture 13 (10/27/09) - Chap. 7 (7.4.2); Chap. 8 (8.2.2a, 8.2.3); Chap. 10 (10.1.2a and c)

Lecture 14 (10/29/09) - Chap. 15 (15.1)

Problem 1 - Consider an n-channel silicon MOSFET and a p-channel silicon MOSFET which are identical in all dimensions and doping level magnitudes except that the gate length, L , of one of the devices is twice that of the other. The K-factors in the large signal characteristics are also identical. [The K-factor is defined as $(W/L)\mu(\epsilon_{ox}/t_{ox})$.]

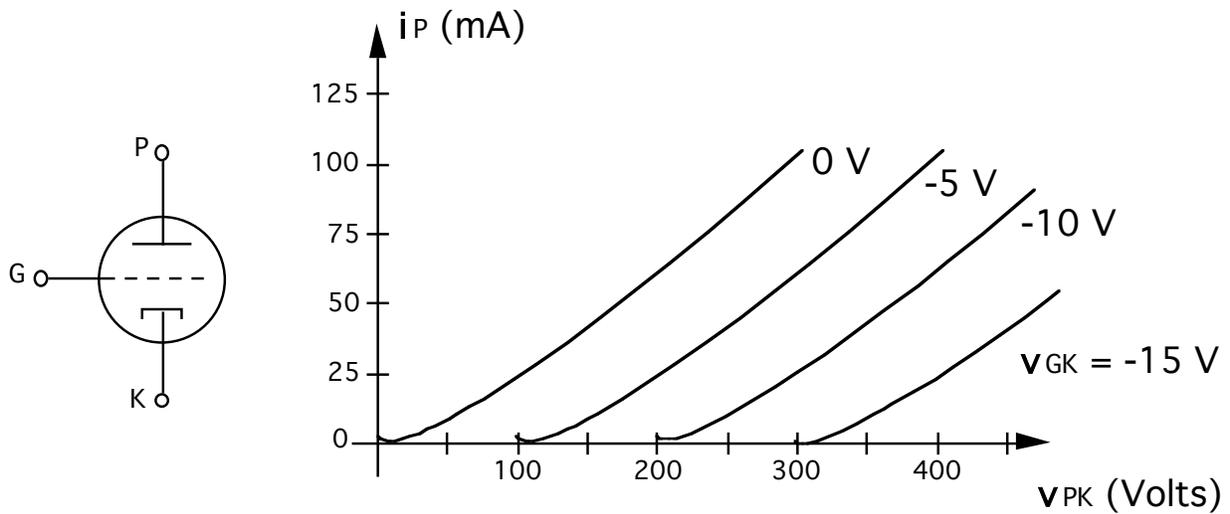
- (i) Which transistor, if either, would you expect to be the one with the longer gate length, and why?
- (ii) What is the ratio of the electron to hole mobility in these transistors (i.e., what is the ratio of the mobility of the electrons in the channel of the n-channel MOSFET to that of the holes in the channel of the p-channel MOSFET)? Explain.
- (iii) Which transistor, if either, has the larger small-signal gate-to-source capacitance in saturation, C_{gs} ? Explain your answer.
- (iv) Which transistor, if either, has the larger small-signal gate-to-drain capacitance in saturation, C_{gd} ? Explain your answer.
- (v) Both transistors are biased in saturation so they have the same magnitude of quiescent drain current, I_D . Which transistor, if either, has the largest small-signal transconductance, g_m ? Explain your answer and estimate the ratio of the two g_m 's.
- (vi) Which transistor, if either, has a larger Early voltage, V_A ? Explain your answer.

Problem 2 - This problem examines and compares (or contrasts) the sub-threshold and strong inversion operation of an n-channel MOSFET like the one we used as the example in Lecture 12. As you will recall, that device had $t_{ox} = 3$ nm and $N_A = 10^{18}$ cm⁻³. This resulted in having $n = \alpha = 1.25$. Assume that the electrostatic potential of the gate metal (degenerately n-doped poly-crystalline silicon) is 0.55 Volts, the channel length is 100 nm, and the electron mobility in the channel is 800 cm²/V-s.

- (a) What are the flat-band and threshold voltages of this device when $v_{BS} = 0$?
- (b) (i) What is the factor γ (which was defined just before Problem 3 on Problem Set 6) for this device? This factor is called the "body factor" and is a gauge of how much the threshold voltage changes with substrate (body) bias, v_{BS} .
 - (ii) What is the threshold voltage if $v_{BS} = -1$ Volt?

- (c) How wide must the gate be to have $K = 1 \text{ mA/V}^2$? (Remember to include α .)
- (d) What is the drain current in saturation when this device is biased 1 Volt above threshold?
- (e) (i) What is the drain current in saturation when this device is biased 0.12 Volts below threshold?
- (ii) What is the drain current in saturation when $v_{GS} = v_{BS} = 0$?
- (iii) How much power is dissipated in an integrated circuit containing 10^6 transistors like this, each in series with a load connecting a 1.5 V power supply buss to ground [as, for example, in Figure 15.2(c) in the course text] when all of the transistors are off with $v_{GS} = 0$?

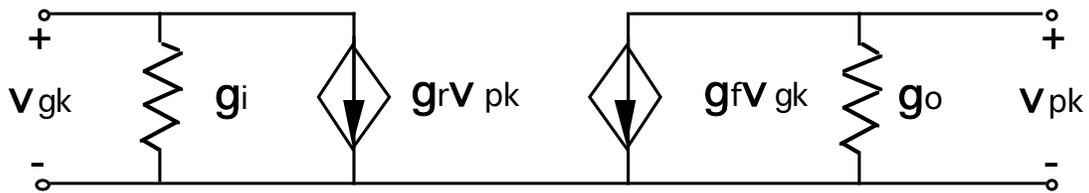
Problem 3 - Several three-terminal devices (e.g., vacuum tube triodes, static induction transistors, field-emitter display pixels) have characteristics like those illustrated below:



$$i_G = I_C(e^{qV_{GK}/kT} - 1) \quad \text{and} \quad i_P = G(M v_{PK} + V_{GK})^{3/2}$$

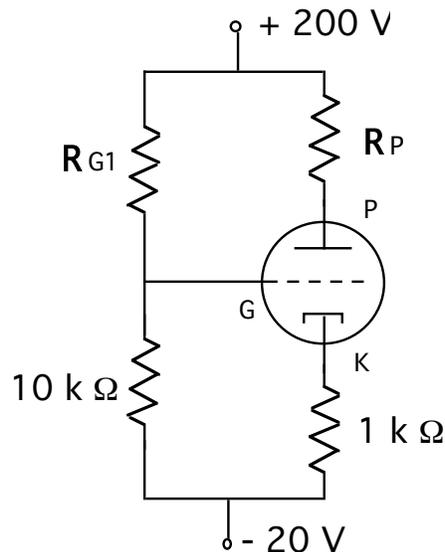
with $G = 2 \text{ mA/V}^{3/2}$, $M = 0.06$, and $I_C = 10^{-6} \text{ A}$

- (a) An incremental model for a device with these characteristics is illustrated below.



Find mathematical expressions for each of the parameters in the incremental model (g_i , g_r , g_f and g_o) and evaluate these expressions at the bias point $V_{GK} = -4 \text{ V}$, and $V_{PK} = 160 \text{ V}$.

(b) This device is biased using the resistor bias circuit illustrated below:



Select R_{G1} and R_P to achieve the bias point specified in Part (a), i.e., $V_{GK} = -4$ V, and $V_{PK} = 160$ V.

Problem 4 (“iLab” problem) - This problem requires that you use a remote-control device measurement and characterization system called “iLab”. Go to <http://ilab.mit.edu>, sign up for a user account if you don’t have one already (this can take a day or two, so sign up well before this problem set is due), and read the user manual provided there. After reading the manual, go to “Launch Lab” and make your measurements using the Java applet that appears.

You select the device that will be under test from the “Device” menu. For this problem use one of the two devices named “3u nMOSFET” (#4 and #6).

Look at the output characteristics of this device as directed below. Prepare and submit the plots requested, and give the requested parameter values.

Caution: Do not let v_{GS} exceed 3 V or v_{DS} exceed 4 V.

- On linear scales, plot i_D vs v_{DS} for $0 \leq v_{DS} < 4$ V, with v_{GS} as a parameter ($0 \leq v_{GS} \leq 3$ V) and with $v_{BS} = 0$. Estimate the threshold voltage, $V_{T'}$, and the Early voltage, $V_{A'}$, for this device.
- Repeat Part (a) with $v_{BS} = -0.5$ V.
- Plot i_D vs v_{GS} , with $v_{DS} = 4$ V and $v_{BS} = 0$ V on a linear scale. Also plot $(i_D)^{1/2}$ vs v_{GS} , and use this plot to find the threshold voltage, $V_{T'}$, and the K-factor of this device with $v_{BS} = 0$.
- Display the plot of i_D vs v_{GS} , with $v_{DS} = 4$ V and $v_{BS} = 0$ V in Part (c) on a log-linear scale and use it to estimate the sub-threshold slope and the value of “n”. Also determine the factor $I_{S,s-t}$ in the expression for sub-threshold current (see, for example, Slide 21 in Lecture 12).

- e) Use the techniques in Parts (c) and (d) to estimate the threshold voltage, sub-threshold slope, the factor $I_{S,S-t}$ and “n” when $v_{BS} = -0.5$ V.

Comment on whether the changes you find from the $v_{BS} = 0$ case have the right sign, and whether they seem reasonable.

- f) Return to your plot of i_D vs v_{DS} for $0 \leq v_{DS} < 4$ V, with v_{GS} as a parameter ($0 \leq v_{GS} \leq 3$ V) and with $v_{BS} = 0$ in Part (a), but only plot it for ($0 \leq v_{GS} \leq V_T$), and make it a log-linear plot, i.e., $\log i_D$ vs v_{DS} . You might even try to make the steps in v_{GS} be nkT/q , and compare your plot to that on Slide 26 of Lecture 12.
- g) Optional extra fun (I am curious to see what you find): Your estimates of K , n , and $I_{S,S-t}$ in Part (d) should all be consistent, and in fact should be related (see Slide 21 of Lecture 12). You should find: $I_{S,S-t} = K_0 (kT/q)^2 (n-1)$. What do you actually find?

Note: The estimates you found in Part (e) should, of course, also be related. You may want to check that too.

Additional final comments on iLab:

The "auto scale" function might be useful for displaying plots.

For research purposes, the system keeps a record of all logins and all scripts that each user executes.

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