Lecture 14 - Digital Circuits (III)

CMOS

October 27, 2005

Contents:

1. Complementary MOS (CMOS) inverter: introduction
2. CMOS inverter: noise margins
3. CMOS inverter: propagation delay
4. CMOS inverter: dynamic power

Reading assignment:

Howe and Sodini, Ch. 5, §5.4

Announcements:

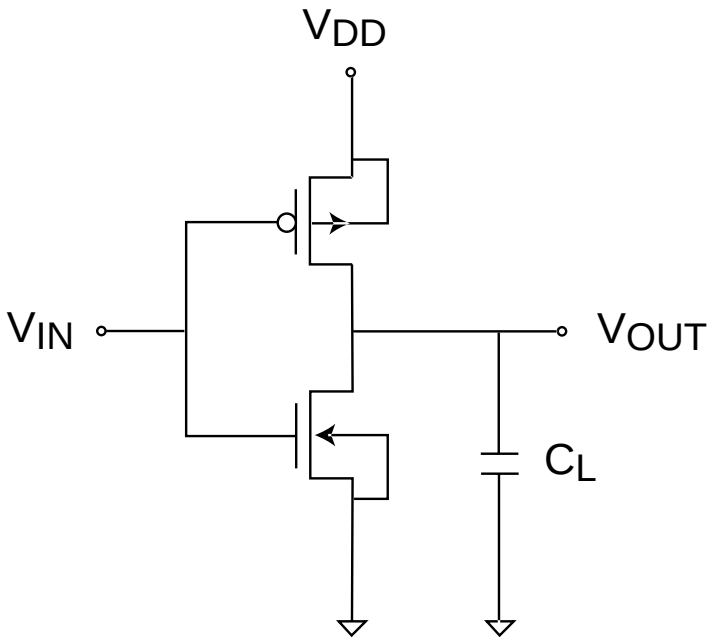
- Cadence tutorial by Kerwin Johnson in place of regular recitations on Friday 10/28

Key questions

- How does CMOS work?
- What is special about CMOS as a logic technology?
- What are the key design parameters of a CMOS inverter?
- How can one estimate the propagation delay of a CMOS inverter?
- Does CMOS burn any power?

1. Complementary MOS (CMOS) Inverter

Circuit schematic:



Basic operation:

- $V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD}$

  $V_{GSn} = 0 < V_{Tn} \Rightarrow$ NMOS OFF

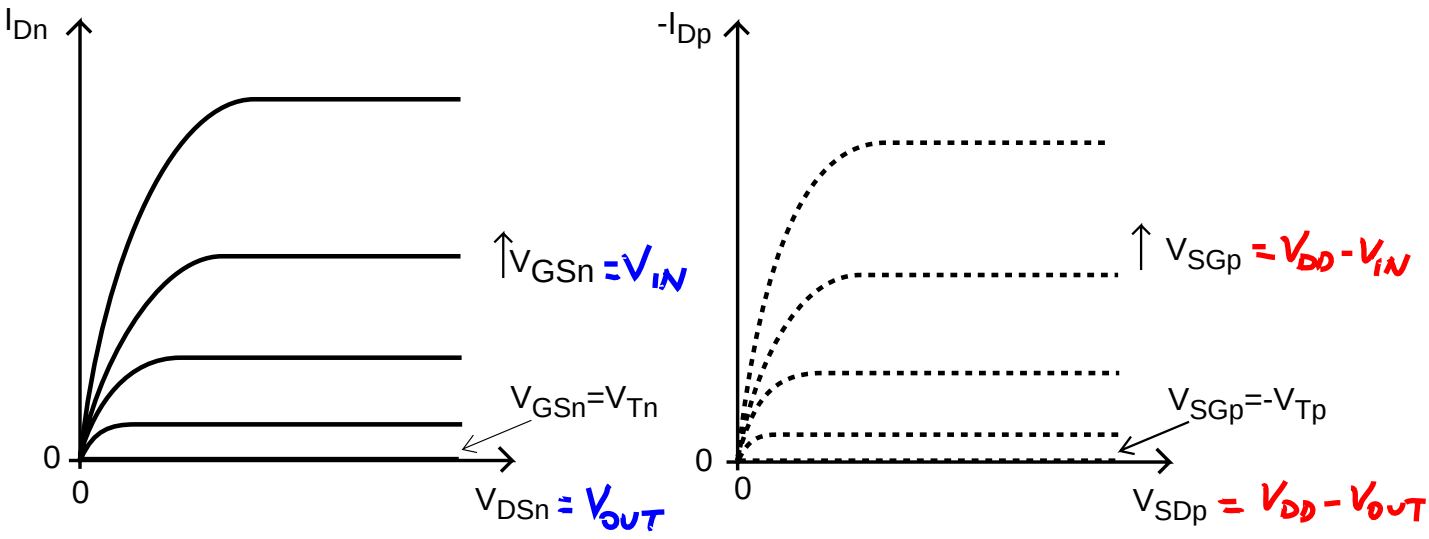
  $V_{SGp} = V_{DD} > -V_{Tp} \Rightarrow$ PMOS ON

- $V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0$

  $V_{GSn} = V_{DD} > V_{Tn} \Rightarrow$ NMOS ON

  $V_{SGp} = 0 < -V_{Tp} \Rightarrow$ PMOS OFF

Output characteristics of both transistors:



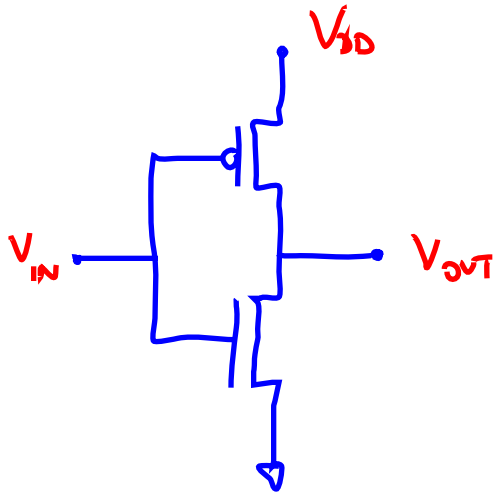
Note:

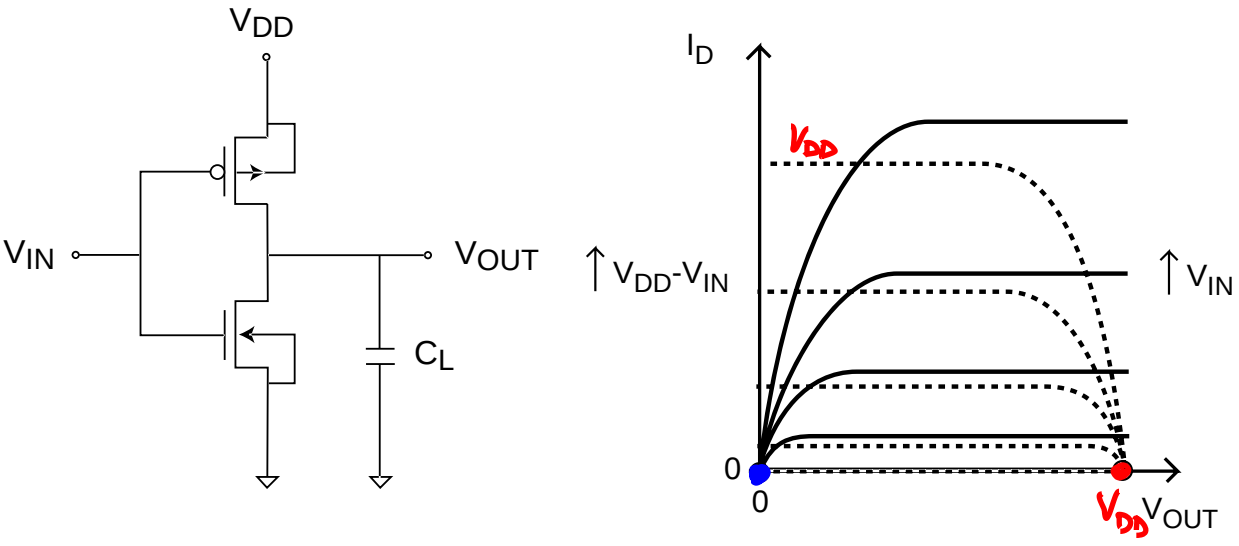
$$V_{IN} = V_{GSn} = V_{DD} - V_{SGp} \Rightarrow \ V_{SGp} = V_{DD} - V_{IN}$$

$$V_{OUT} = V_{DSn} = V_{DD} - V_{SDp} \Rightarrow \ V_{SDp} = V_{DD} - V_{OUT}$$

$$I_{Dn} = -I_{Dp}$$

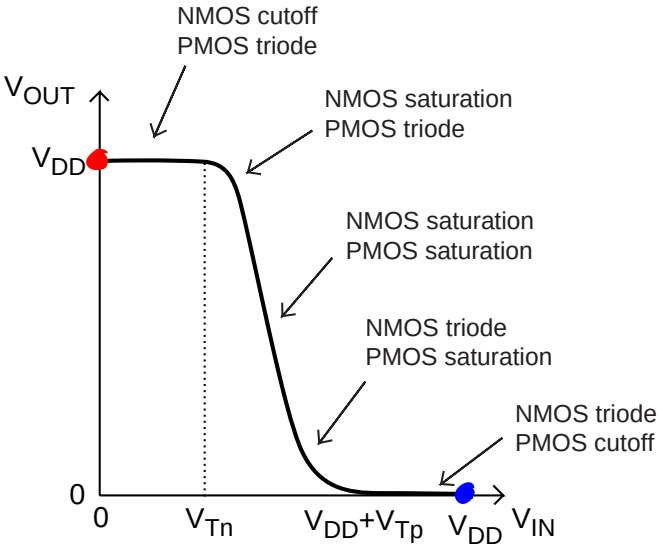
Combine into single diagram of I_D vs. V_{OUT} with V_{IN} as parameter.





⋆ *no current while idling in any logic state.*

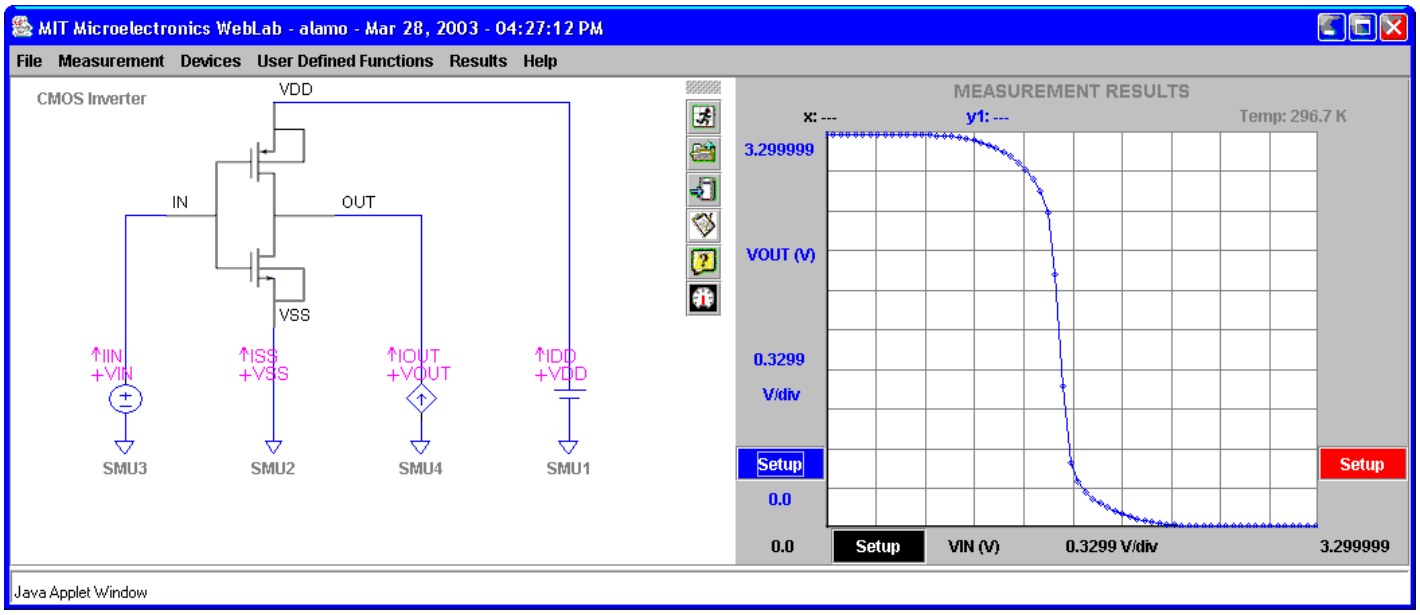
Transfer function:



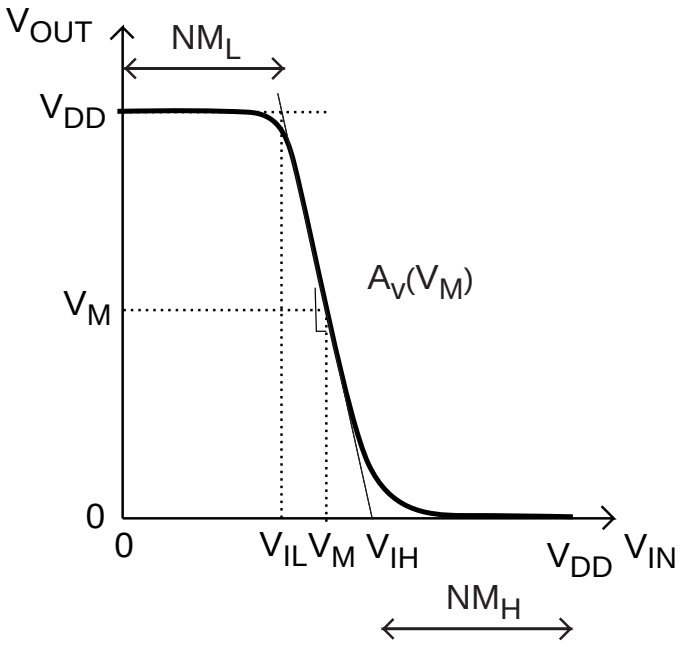
⋆ *"rail-to-rail" logic: logic levels are* 0 *and* V_{DD}

⋆ *high* $|A_v|$ *around logic threshold* $\Rightarrow$ good noise margins

Transfer characteristics of CMOS inverter in WebLab:



2. CMOS inverter: noise margins



- Calculate V_M
- Calculate $A_v(V_M)$
- Calculate NM_L and NM_H

□ Calculate V_M ($V_M = V_{IN} = V_{OUT}$)

At V_M both transistors saturated:

$V_{GSn} = V_{IN}$

$$I_{Dn} = \frac{1}{2}\frac{W_n}{L_n}\mu_n C_{ox}(V_M - V_{Tn})^2$$

$$-I_{Dp} = \frac{1}{2}\frac{W_p}{L_p}\mu_p C_{ox}(V_{DD} - V_M + V_{Tp})^2$$

$V_{SGp} = V_{DD} - V_{IN}$

Define:

$$k_n = \frac{W_n}{L_n}\mu_n C_{ox}, \quad k_p = \frac{W_p}{L_p}\mu_p C_{ox}$$

Since:

$$I_{Dn} = -I_{Dp}$$

Then:

$$\frac{1}{2}k_n(V_M - V_{Tn})^2 = \frac{1}{2}k_p(V_{DD} - V_M + V_{Tp})^2$$

Solve for V_M:

$$\boxed{V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}}$$

Usually, V_{Tn} and V_{Tp} fixed and $V_{Tn} = -V_{Tp}$

$\Rightarrow$ V_M engineered through k_p/k_n ratio

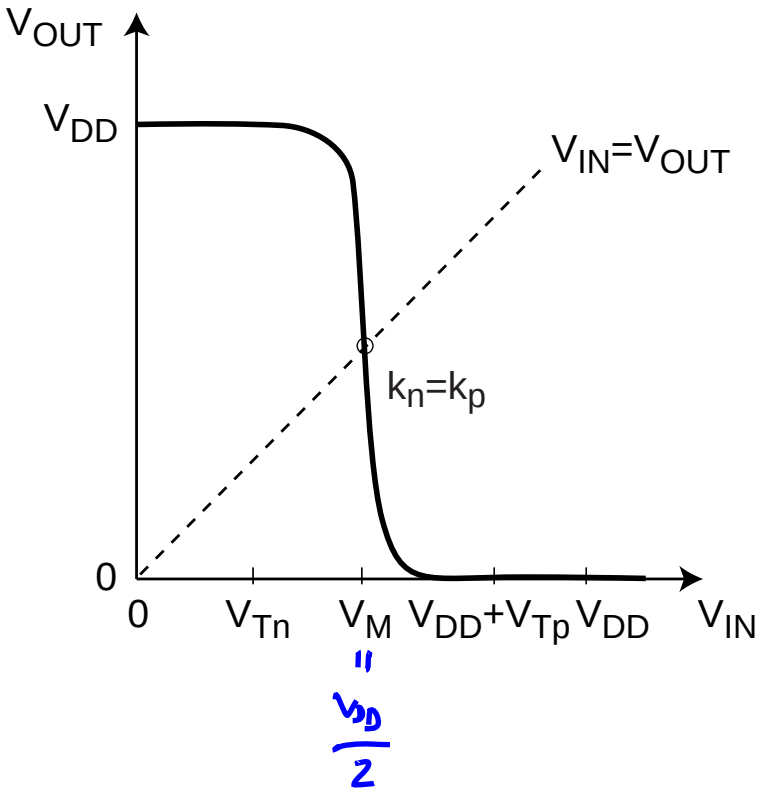
- Symmetric case: $k_n = k_p$

$$V_M = \frac{V_{DD}}{2}$$

This implies:

$$\frac{k_p}{k_n} = 1 = \frac{\frac{W_p}{L_p}\mu_p C_{ox}}{\frac{W_n}{L_n}\mu_n C_{ox}} \simeq \frac{\frac{W_p}{L_p}\mu_p}{\frac{W_n}{L_n} 2\mu_p} \Rightarrow \frac{W_p}{L_p} \simeq 2\frac{W_n}{L_n}$$

Since usually $L_p \simeq L_n \Rightarrow W_p \simeq 2W_n$.



- Asymmetric case: $k_n \gg k_p$, or $\frac{W_n}{L_n} \gg \frac{W_p}{L_p}$

$$V_M \simeq V_{Tn}$$

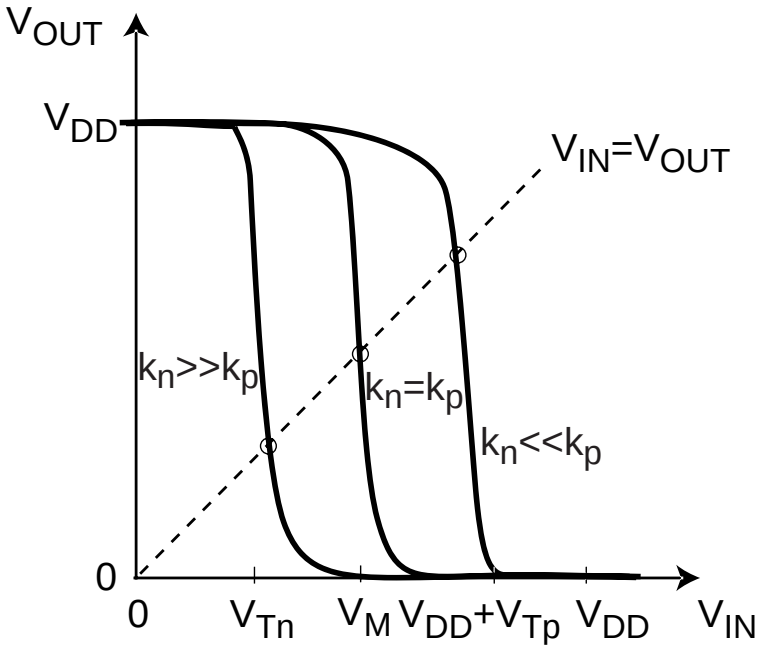
NMOS turns on as soon as V_{IN} goes above V_{Tn}.

- Asymmetric case: $k_n \ll k_p$, or $\frac{W_n}{L_n} \ll \frac{W_p}{L_p}$

$$V_M \simeq V_{DD} + V_{Tp}$$

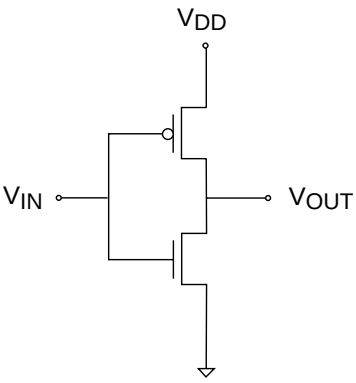
PMOS turns on as soon as V_{IN} goes below $V_{DD} + V_{Tp}$.

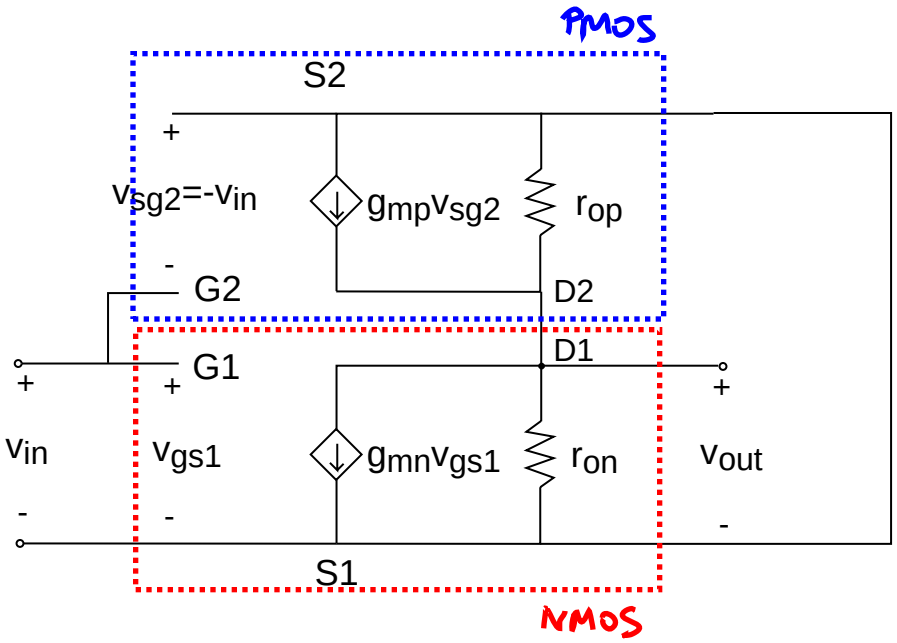
Can engineer V_M anywhere between V_{Tn} and $V_{DD} + V_{Tp}$.

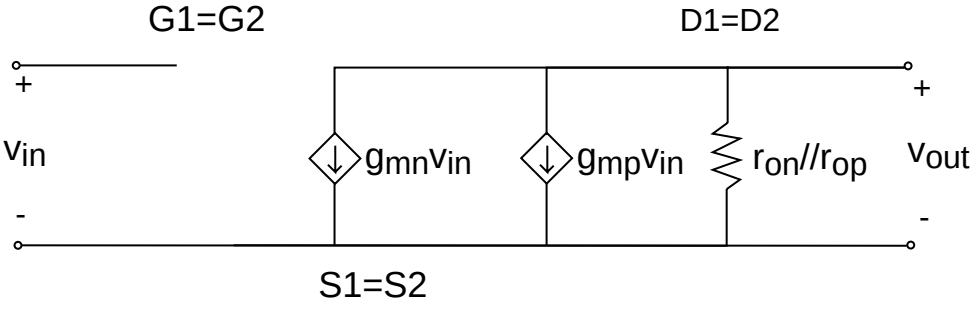


□ Calculate $A_v(V_M)$

Small-signal model:



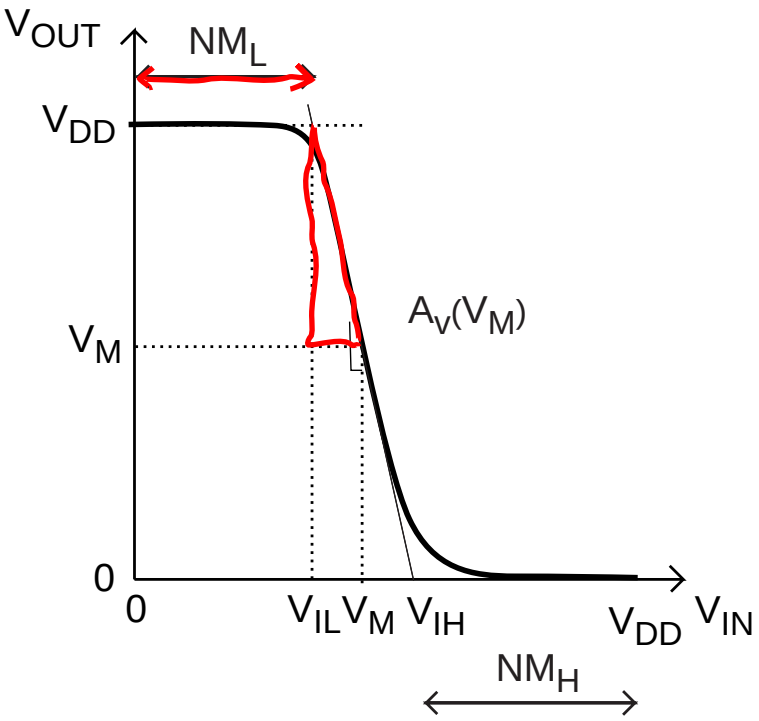




$$A_v = -(g_{mn} + g_{mp})(r_{on}//r_{op})$$

This can be rather large.

□ Noise margins



- Noise-margin-low:

$$V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

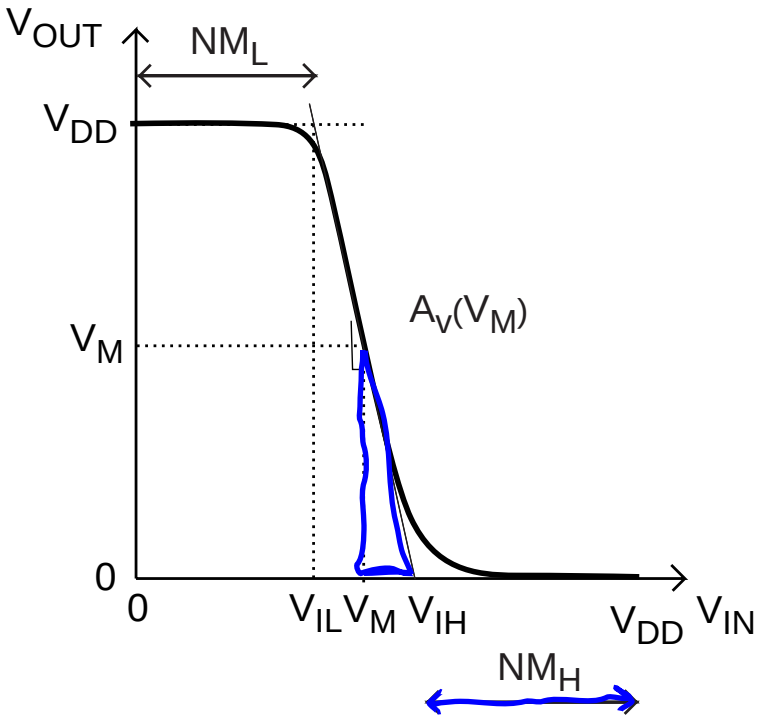
Therefore:

$$NM_L = V_{IL} - V_{OL} = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

In the limit of $|A_v| \to \infty$:

$$NM_L \to V_M$$

- Noise-margin-high:



$$V_{IH} = V_M(1 + \frac{1}{|A_v|})$$

and

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_M(1 + \frac{1}{|A_v|})$$

In the limit of $|A_v| \to \infty$:

$$NM_H \to V_{DD} - V_M$$

When $V_M = \frac{V_{DD}}{2}$ $\Rightarrow$ $\boxed{NM_L = NM_H = \frac{V_{DD}}{2}}$

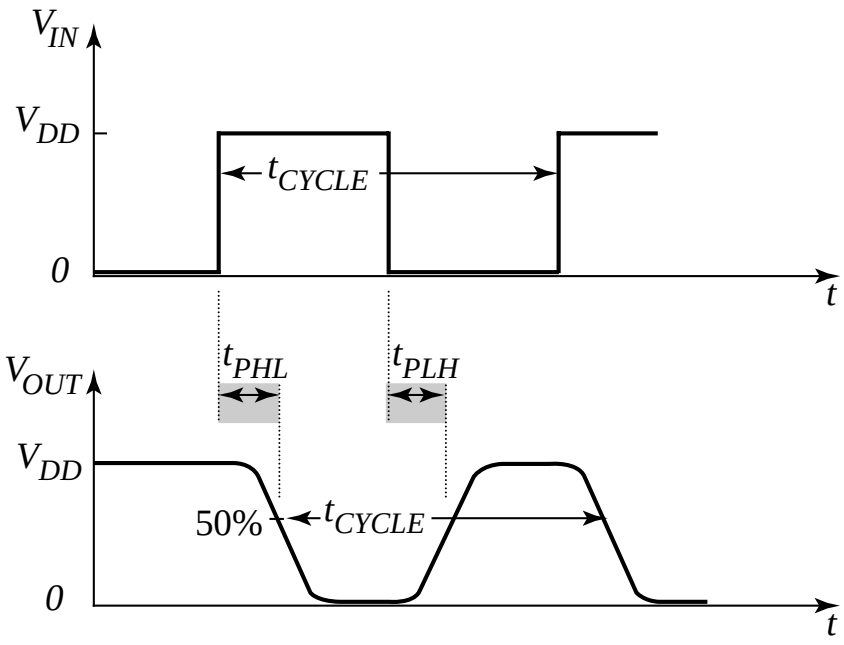
3. CMOS inverter: propagation delay

Inverter propagation delay: time delay between input and output signals; key figure of merit of logic speed.

Typical propagation delays: $< 1\ ns$.

Complex logic system has 20-50 propagation delays per clock cycle.

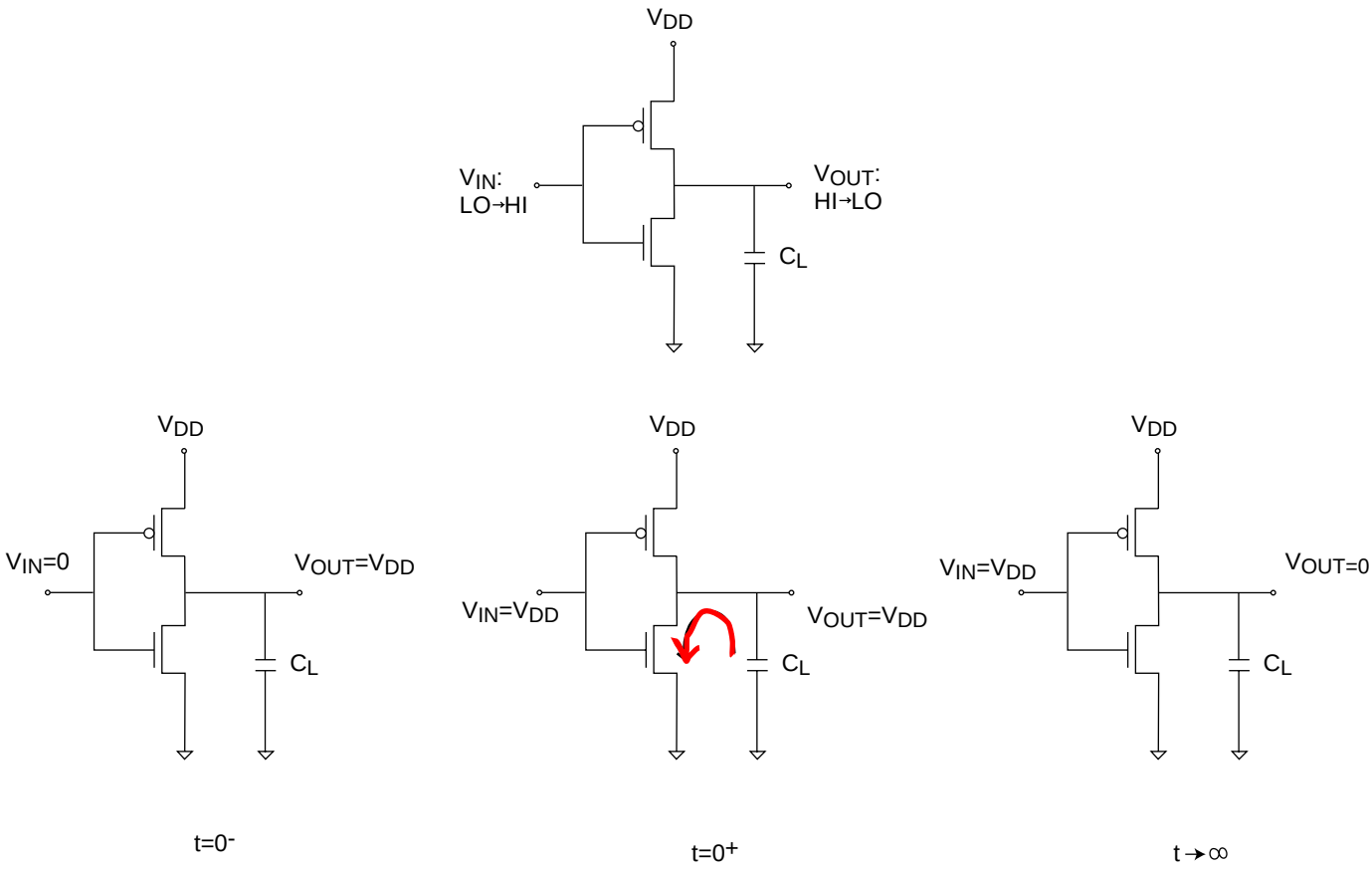
Estimation of t_p: use square-wave at input



Average propagation delay:

$$t_p = \frac{1}{2}(t_{PHL} + t_{PLH})$$

□ Propagation delay high-to-low:



During early phases of discharge, NMOS is saturated and PMOS is cut-off.

Time to discharge *half* of C_L:

$$t_{PHL} \simeq \frac{\frac{1}{2}\text{charge of } C_L @ t = 0^-}{\text{discharge current @ } t = 0^+}$$

Charge in C_L at $t = 0^-$:

$$Q_L(t = 0^-) = C_L V_{DD}$$

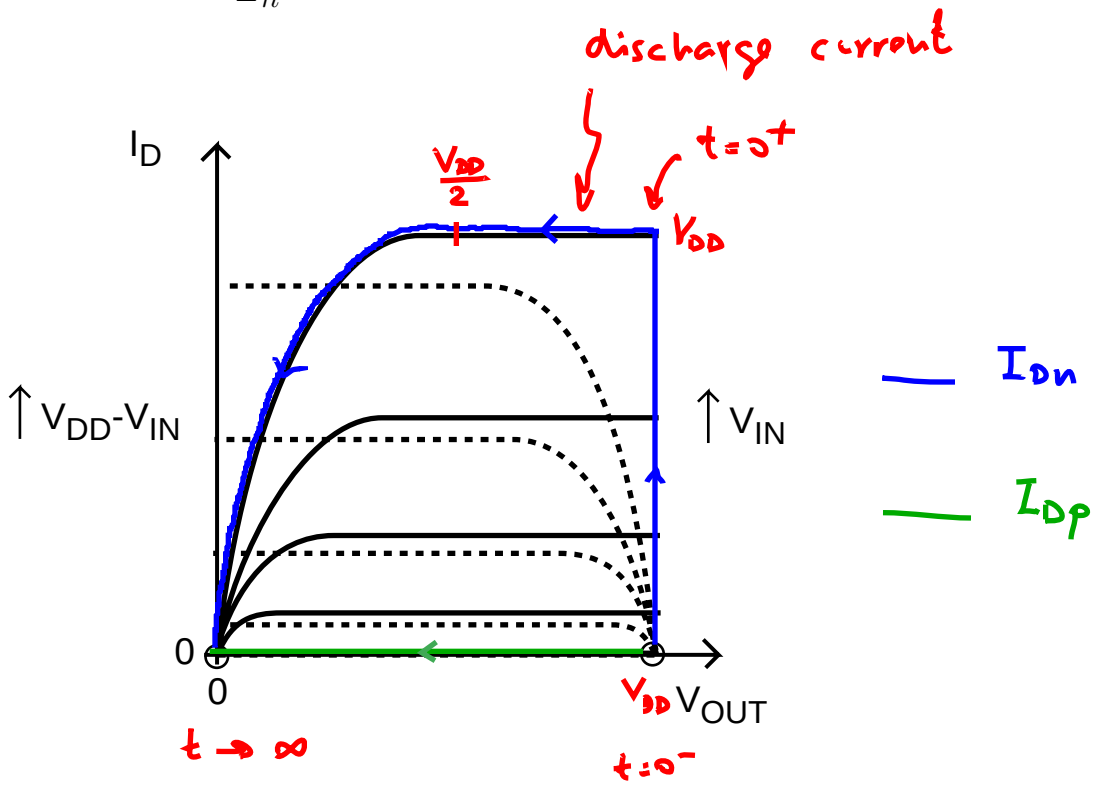
Discharge current (NMOS in saturation):

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}(V_{DD} - V_{Tn})^2$$

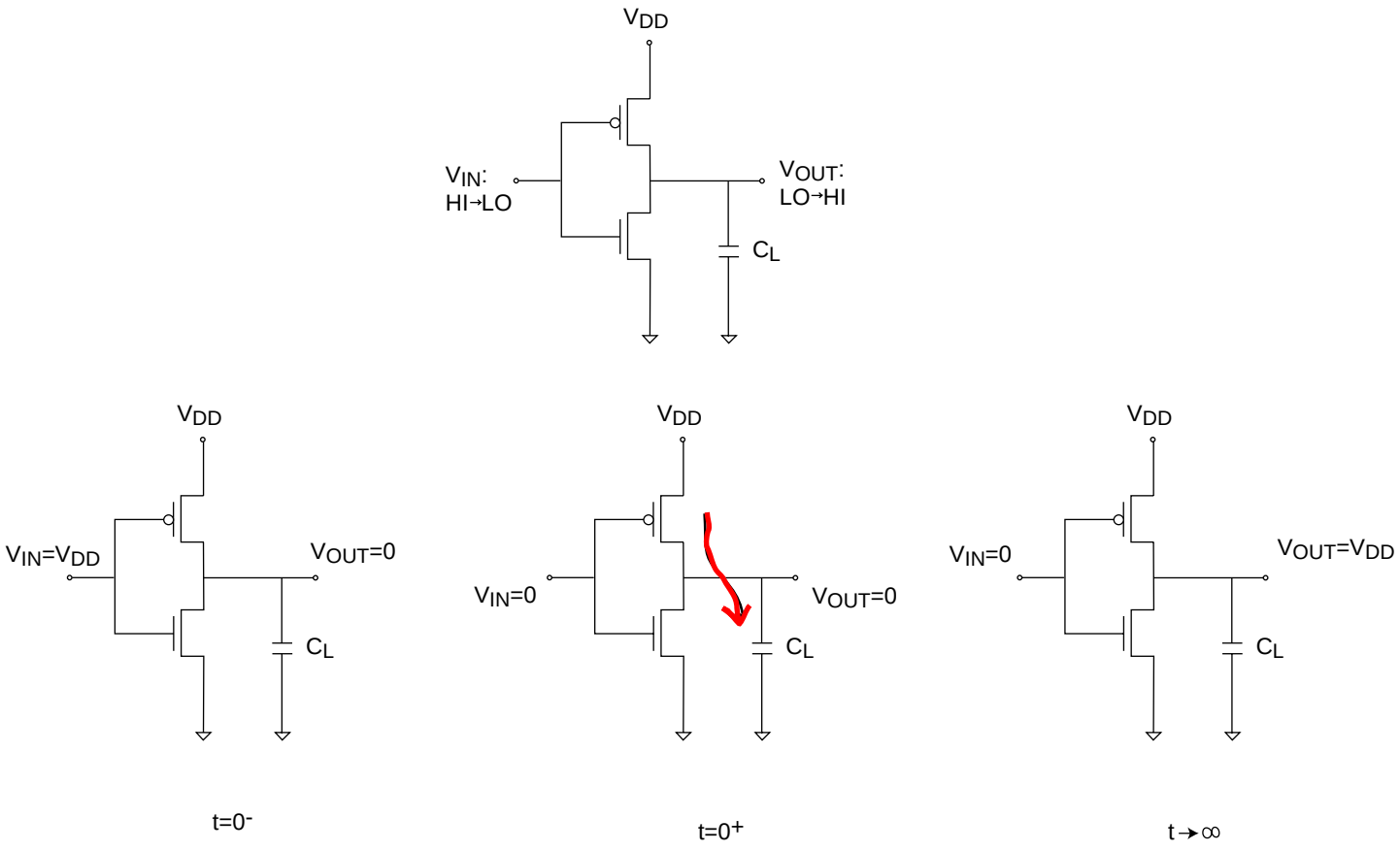
($t = 0^+$) $V_{GSn} = V_{IN}$

Then:

$$t_{PHL} \simeq \frac{C_L V_{DD}}{\frac{W_n}{L_n}\mu_n C_{ox}(V_{DD} - V_{Tn})^2}$$



□ Propagation delay low-to-high:



During early phases of charge, PMOS is saturated and NMOS is cut-off.

Time to charge *half* of C_L:

$$t_{PLH} \simeq \frac{\frac{1}{2}\text{charge of } C_L @ t = \infty}{\text{charge current } @ t=0^+}$$

Charge in C_L at $t = \infty$:

$$Q_L(t = \infty) = C_L V_{DD}$$

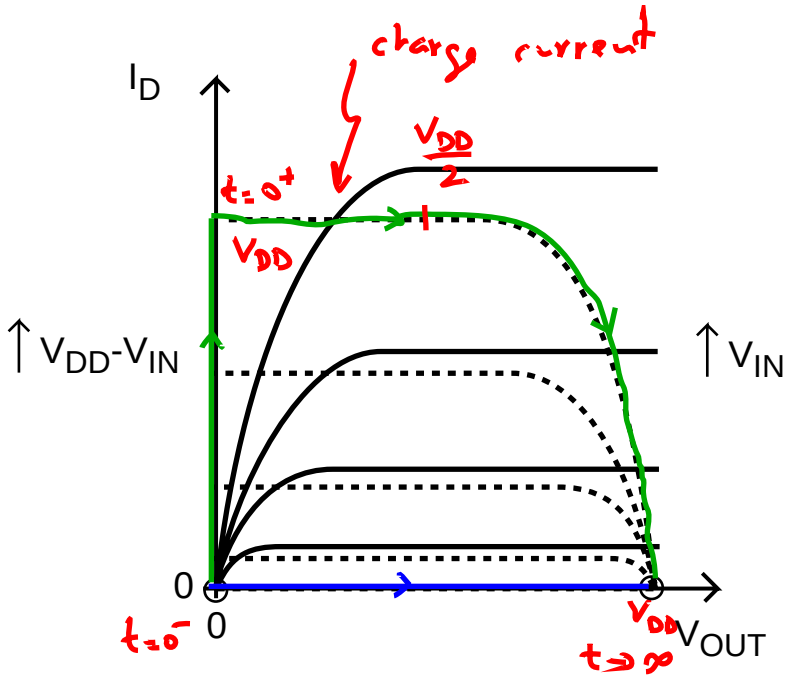
Charge current (PMOS in saturation):

$$-I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}(V_{DD} + V_{Tp})^2$$

$(t=0^+)$ $V_{SGp} = V_{DD} - V_{IN} = V_{DD}$

Then:

$$t_{PLH} \simeq \frac{C_L V_{DD}}{\frac{W_p}{L_p}\mu_p C_{ox}(V_{DD} + V_{Tp})^2}$$



Key dependencies of propagation delays:

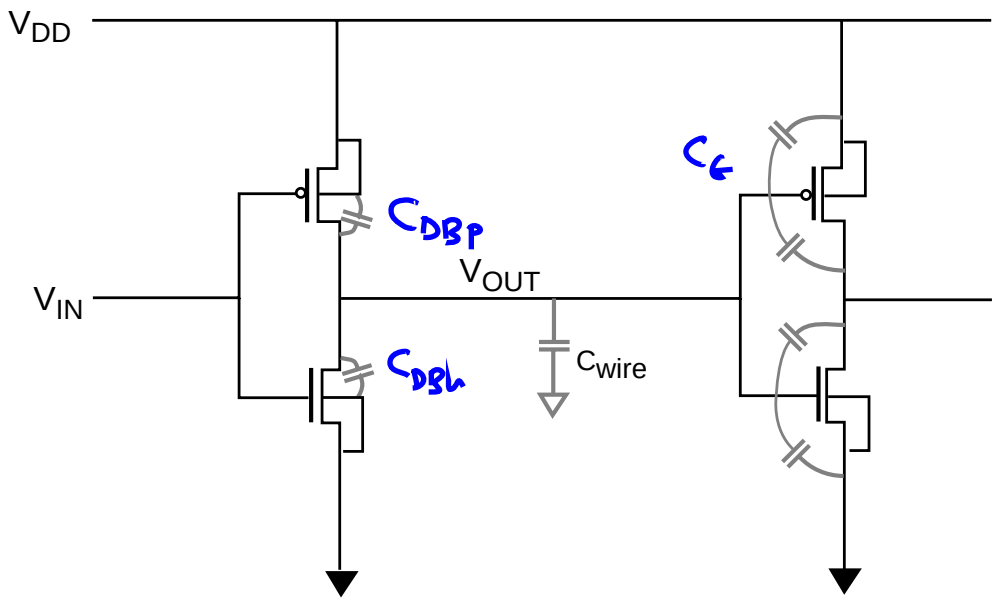
- $V_{DD} \uparrow \Rightarrow t_p \downarrow$
  Reason: $V_{DD} \uparrow \Rightarrow Q(C_L) \uparrow$, but also $I_D \uparrow$
  Trade-off: $V_{DD} \uparrow$, more power usage.

- $L \downarrow \Rightarrow t_p \downarrow$ → motivation for scaling !
  Reason: $L \downarrow \Rightarrow I_D \uparrow$
  Trade-off: manufacturing costs!

Components of load capacitance C_L:

- *following logic gates*: must add capacitance presented by each gate of every transistor the output is connected to
- *interconnect wire* that connects output to input of following logic gates
- *own drain-to-body capacitances*

$$C_L = C_G + C_{wire} + C_{DBn} + C_{DBp}$$



[See details in Howe & Sodini §5.4.3]

4. CMOS inverter: dynamic power

• In any of the two logic states: one transistor always OFF ⇒ zero static power dissipation.

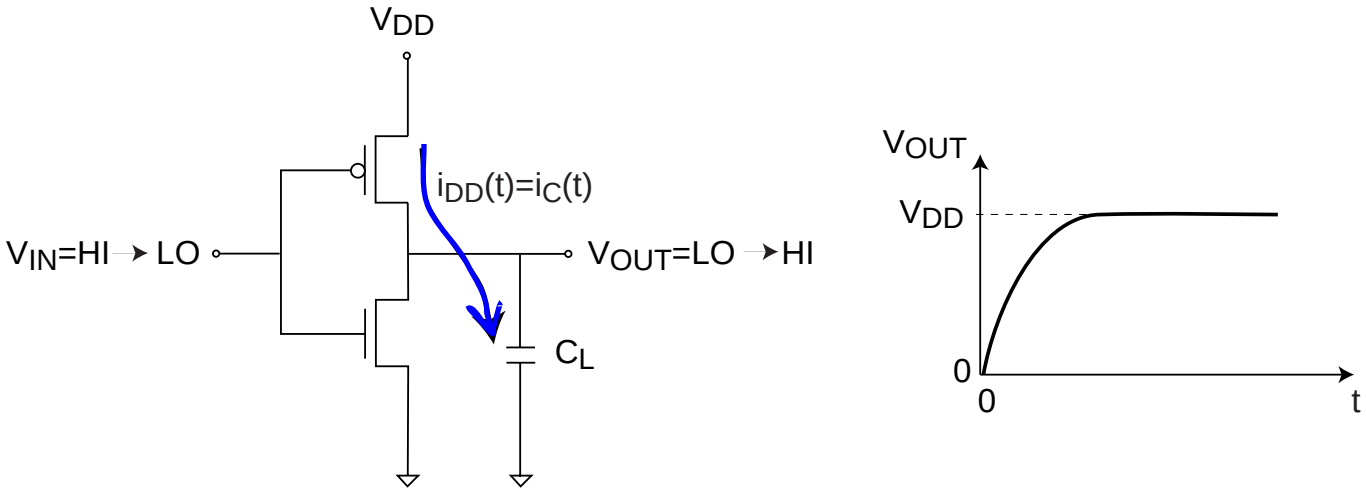
• Dynamic power?

Every complete transient, C_L is charged up to V_{DD} and then discharged to 0

⇒ energy dissipated

⇒ clock frequency ↑ ⇒ dissipated power ↑

☐ Dynamic power dissipated while charging load



1. Energy provided by battery during transient:

$$E_S = \int_0^\infty V_{DD} i_C(t) dt = V_{DD} \int_0^\infty C_L \frac{dv_{OUT}}{dt} dt =$$
$$= C_L V_{DD} \int_0^{V_{DD}} dv_{OUT} = C_L V_{DD}^2$$

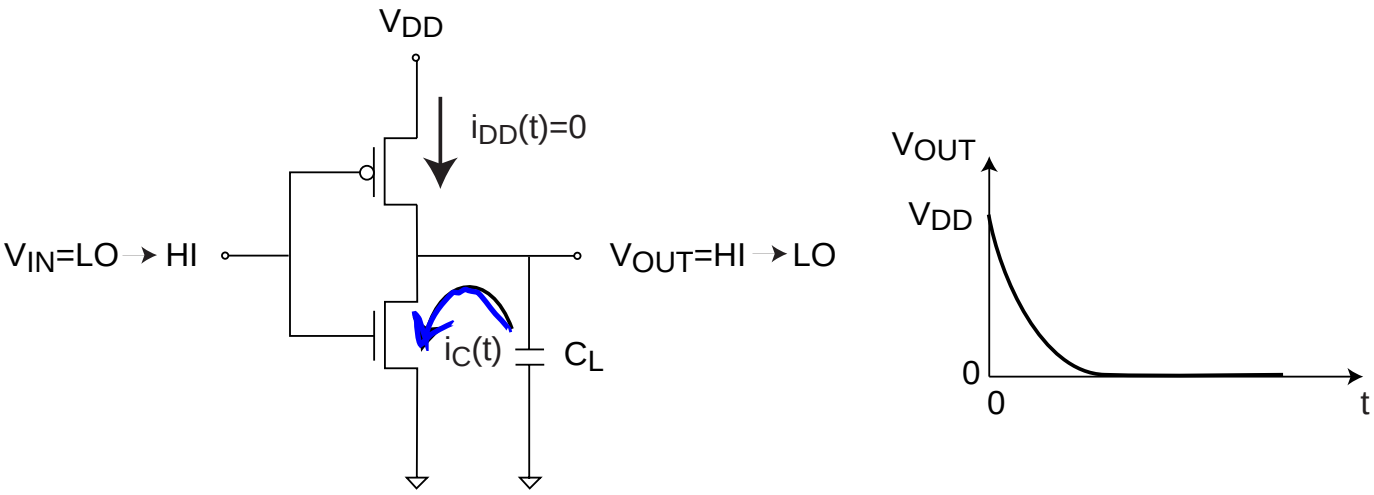
2. Energy stored in capacitor during transient:

$$\Delta E_C = E_C(t=\infty) - E_C(t=0) = \frac{1}{2} C_L V_{DD}^2$$

3. Energy dissipated in PMOS during transient:

$$E_P = E_S - \Delta E_C = \frac{1}{2} C_L V_{DD}^2$$

□ Dynamic power dissipated while discharging load



1. Energy provided by battery during transient:

$$E_S = \int_0^\infty V_{DD} i_{DD}(t) dt = 0$$

2. Energy removed from capacitor during transient:

$$\Delta E_C = E_C(t=0) - E_C(t=\infty) = \frac{1}{2} C_L V_{DD}^2$$

3. Energy dissipated in NMOS during transient:

$$E_N = \Delta E_C = \frac{1}{2} C_L V_{DD}^2$$

☐ Energy dissipated in complete cycle

**

$$E_D = E_P + E_N = \Sigma E_S = C_L V_{DD}^2$$

☐ Power dissipation

If complete switching cycle takes place f times per second:

***

$$P_D = f E_D = f C_L V_{DD}^2$$

Fundamental trade-off between switching speed ant power dissipation!

Key dependencies in dynamic power:

- $f \uparrow \Rightarrow P_D \uparrow$, charge and discharge C_L more frequently
- $C_L \uparrow \Rightarrow P_D \uparrow$, more charge being shuttled around
- $V_{DD} \uparrow \Rightarrow P_D \uparrow$, more charge being shuttled around

Key conclusions

- Key features of CMOS inverter:
  - no current while idling in any logic state
  - "rail-to-rail" logic: logic levels are 0 and V_{DD}
  - high $|A_v|$ around logic threshold $\Rightarrow$ good noise margins

- CMOS inverter logic threshold and noise margins engineered through W_n/L_n and W_p/L_p.

- Key dependences of propagation delay:
  - $V_{DD} \uparrow \Rightarrow\ t_p \downarrow$
  - $L \downarrow \Rightarrow\ t_p \downarrow$

- Dynamic power dissipated in CMOS:

$$P_D = f E_D = f C_L V_{DD}^2$$

  Fundamental trade-off between switching speed and power dissipation.